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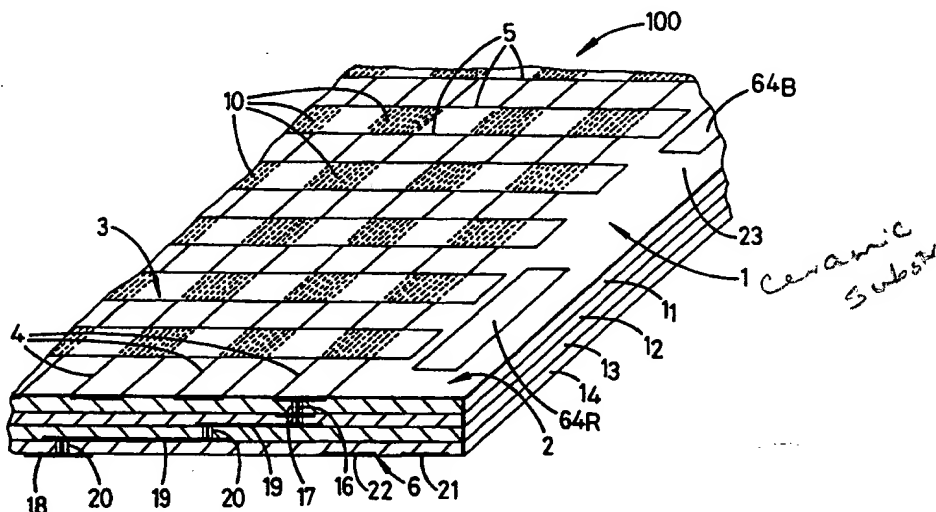
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(54) Title: **VISUAL DISPLAY**



(57) Abstract

A field effect emission device (100) for a visual display has a ceramic substrate (1). On an emission side (2) of the substrate, it has an emission layer (3) including a lattice of conductive emitter and gates line stripes (4, 5). For electrical connection to the emitter and gate stripes, the substrate has apertures (16), into which the strip material - or other conductive material - extends as vias (17). The device substrate is made up of several substrate layers 11, 12, 13, 14 bonded together. Each layer piece has connection strips (19) set into its opposite surfaces and interconnecting vias (20), of the same material as the strips. The connection strips of adjacent layers about or at least vias of one layer abut with the connection strips of the next layer, providing electrical contact. The connection strips and the vias are arranged to spread or fan out the connections from the stripe pitch, typically 0.0125'', to that of driver chip contacts, typically 0.050'', to be connected to the contact pads (18).

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VISUAL DISPLAY

Field of the Invention

The present invention relates to a visual display, particularly though not exclusively for use with data processing apparatus.

5

Background of the Invention

Visual displays for data processing apparatus, such as computers, are normally of the cathode ray tube type. These generally have a depth of the order of their size dimension, which conventionally is their corner to corner or diagonal
10 dimension. This depth can render them inconvenient in use. Recently, laptop computers have become increasingly widely used. These incorporate a "flat" screen display, usually of the liquid crystal type.

Proposals have been made to provide displays having flat screen cathode ray
15 tubes. These are known as Spindt cathodes, after the inventor of US Patent No. 3,755,704. In this specification, they are referred to as field emission devices.

Object of the Invention

The object of the present invention is to provide an improved "flat" screen
20 field emission visual display and an emission device for the display.

This application claims priority from our UK application No. 9720723.7 of 1st October 1997 and U.S. Provisional application No. 60/067,508 of 4 December 1997. The priority applications describe both our field emission device invention
25 and its manner of sealing into a display and a machine therefor. This specification describes both aspects and claims our field emission device invention. A copending application filed on the same date herewith (PCT Serial No. _____) similarly describes both aspects and claims the sealing invention.

The Invention

30 According to a first aspect of the invention there is provided a field effect emission device for a visual display comprising:
a substrate and

- an emission layer on one face of the substrate, the emission layer having:
 - a multiplicity of emitters and gates, arranged as an array of emission pixels and
 - conductive connections in the emission layer to the emitters and the gates;
- 5 • the substrate having:
 - conductive vias provided through the substrate or at least a front layer thereof to at least some of the said conductive connections in the emission layer for electrical connection to their emitters and gates.

10 We envisage that normally all of the conductive connections in the emission layer will have respective vias.

Provision of the conductive vias to the conductive connections in the emission layer provides direct contact to the connections and thus to the emitters and the gates.
15 This has advantages in terms of the real time response of the emitters and gates to control signals. In other words, it provides for fast switching of the emitters and gates and thus sharp video characteristics.

Normally, the conductive connections will be emitter and gate lines to which
20 the vias connect directly.

In preferred embodiments, each of the emitter and gate lines has a plurality of vias connected to it.

25 Whilst it is envisaged that some of the vias may connect to their lines at their ends; preferably the vias are provided within the body of emitters or the gates, that is with emitters or gates positioned on the lines to both sides of the position of the vias.

In accordance with an important feature of the invention, the drivers are
30 mounted on the back face (the face opposite from the emitter face) of the substrate. Again, in combination with the vias through the substrate this enhances emission response.

It is envisaged that the substrate can have a single layer, with electrical connection tracks and preferably driver contact pads provided on its face opposite from the emission layer.

5 Normally, the substrate has at least one substrate layer additional to the front substrate layer,

- the or each said additional substrate layer having conductive vias therethrough,
- electrical interconnection tracks being provided at the interface(s) between the or each adjacent pair of substrate layers for electrical interconnection of the vias of
10 the pair(s) of adjacent layers and
- electrical connection tracks and preferably driver contact pads being provided on an outer face of a back one of the additional substrate layer(s) opposite from the front substrate layer.

15 This arrangement provides that the pitch of the gate and emitter lines can be progressively fanned out for connection to drivers.

20 Additionally, the field emission device will usually include at least one intermediate, additional substrate layer between the front and the back substrate layers.

The electrical interconnection tracks provided at the interface(s) between the or each adjacent pair of substrate layers can be provided on one only of the respective substrate layers at the interface(s), inter-layer contact being between vias of one layer and tracks of the other layer. Alternatively, the electrical interconnection tracks can
25 be provided on both of the respective substrate layers at the interface(s), inter-layer contact being between tracks of one layer and tracks of the other layer.

30 Preferably, no gate line nor emitter line connection via is coincident, from the front substrate layer to the next, with a via in the next substrate layer

Preferably, the gate line and emitter line vias are arranged in at least the substrate layer having the emission layer in an array of aligned series of vias in two alternate orientations, both orientations being offset with respect to the emitter and

gate line directions within the array, all the series are parallel to one or other of the orientations. The array of aligned series of vias can be a zig zag array with gaps between the zigs and the zags. In one particular arrangement, one of the alternate orientations is equal to the orientation of the aligned series, and alternate series of vias
5 are not only parallel but themselves aligned.

The substrate is preferably of ceramic, conveniently of alumina to provide compatibility of thermal expansion with other components of the visual display, particularly a face plate. The vias are apertures in the substrate layers, which are
10 filled with sintered metallic material.

At least some of the electrically conductive connections, lines, connection tracks and interconnection tracks are locally recessed into the material of the substrate layer(s). In particular, the emitter lines are preferably flush on their emission sides
15 with the emission side of the substrate, with a planar dielectric layer separating the emission lines and the gates lines. Normally, a resistive layer will be provided on the emitter line side of the dielectric layer.

In one embodiment, the substrate includes additional vias and conductive
20 tracks for providing electric connection through the substrate for phosphor excitation lines.

*vias
for
anode
plate*

In accordance with a further preferred feature, the back face of the substrate has a peripheral metallic stripe for solder connection of the device into the visual
25 display.

Further, power and signal supply tracks are preferably provided on the back
surface of the back layer for powering the drivers and providing control signals to
them.

30

Normally, the gates are circular apertures in the gate line stripes, with the emitters being pointed features projecting towards the gate apertures through voids in the dielectric layer.

According to a second aspect of the invention there is provided a visual display comprising:

- a field emission device of the first aspect;
- anode* • a glass face plate incorporating phosphor material selectively excitable by the emission device pixels; and
- fused sealing material peripherally sealing the face plate to the emission device, whereby the face plate is parallelly spaced from the emission layer of the emission device and the space therebetween is evacuated.

10 It can be envisaged that the sealing material is interposed directly between the face plate and the emission device. However, it is preferred that the sealing material is provided on a wall interposed between the face plate and the emission device.

15 In the preferred embodiments, the visual display includes a carrier attached to the face of the emission device opposite from its emission layer.

The preferred arrangement is that the fused sealing material is provided on a peripheral wall which is sealed to the carrier and extends from it to the face plate or which forms one limb of the carrier which is of L-shaped cross-section and extends 5 towards the face plate, the face plate being sealed to the wall by the fused sealing material and the emission device being sealingly attached to the carrier at the face of the emission device opposite from its emission layer. *d. 2, 3*

25 Whilst the emission device may be secured to the carrier by means of adhesive, in the preferred embodiments, the device is soldered to the carrier. *4*

Preferably, the emission device and the peripheral, carrier wall are complementarily shaped, for locating the emission device on the carrier. In one embodiment, the peripheral, carrier wall defines a space into which the emission device fits with negligible gap between the emission device and the wall. In another 30 embodiment, the peripheral, carrier wall defines a space which is larger than the emission device, one of the wall and the emission device, preferably the latter, having

projections for engaging with the other, for location of the emission device, a gap being present between the wall and the emission device between the projections.

18 Since the emission device will have electronic components soldered to it, the soldering of the carrier is preferably effected with high temperature solder. For this, mating portions of the device and the carrier are provided with complementary metallic tracks, to one of which the solder is preliminarily applied. The back layer of the ceramic substrate and the carrier can include metallic tracks also connected by high temperature solder for electric power and drive signal connection to the device.
10 Alternatively to this, connectors may be attached directly to the ceramic substrate in the manner of the drivers to be described below.

2 The carrier is preferably of the same material as the ceramic substrate, particularly to provide a similar coefficient of thermal expansion. Further, the carrier is preferably of laminated construction. As an alternative, the carrier may be of high temperature plastics material.

21 The sealing means preferably comprises fused glass frit between the face plate and the carrier. The frit can have sloping sides. Conveniently this is provided by shaping it to a trapezoidal cross-section. The advantage of this shape is that it enables a gap at the frit to be bridged. 24

To support the face plate against collapse towards the emission device, an array of spacers is preferably provided between the face plate and the emission layer.
25 Conveniently the spacers can be secured to the face plate. They may be of glass, ceramic or high temperature plastics material. Spacers may be provided peripherally - of the phosphor material on the face plate and the emission array on the substrate - or within the area of the phosphor material and the emission array, that is the active area of the visual display. Such spacers are referred to as "outer spacers" and "inner spacers" respectively. Preferably, some at least of the outer spacers can carry contact tracks for the phosphor excitation lines, whereby the phosphor pixels can be excited by drivers carried on the emission device. Where the arrangement of the inner spacers causes them to attract electron flow from the emitters, the former may carry an electrical track, which has a voltage applied to it in use, causing the electrons to be

repelled to continue towards the phosphor material. Preferably, the inner spacers are set in grooves in the emission layer and in a layer on the face plate including the phosphor material layer.

5 The inner spacers may extend across the full width of the active area. Alternatively, they may be provided as short lengths and/or crosses. Whilst it is possible that the inner spacers may be of a width to obscure one or more lines of emission pixels, the preferred inner spacers are thin in comparison with the pixel line spacing, whereby they do not interfere with any of the pixels. For this, they may also
10 have a tapered cross-section, being thinner at their face plate edge. The outer spacers can be thicker, particularly where they are providing connection to the phosphor excitation lines.

 For a small display, a single emission device only may be provided in the
15 display. For larger displays, a plurality of laterally abutted emission devices may be provided, all mounted on a common carrier. Preferably, the emission devices are dimensioned at abutting edges for pixel alignment and at peripheral edges for abutment with the peripheral carrier wall. The carrier has additional members bridging the side members of the carrier. The emission devices are supported and
20 sealed at abutting edges by the bridging members. The bridging members and the emission devices are provided with complementary solder contacts for providing electrical contact between the circuitry of the adjacent emission devices. Conveniently this is provided at local swellings in the width of the bridging members, with sealing solder tracks following the edges of the bridging members and the solder
25 contacts being provided between the solder tracks.

 Preferably, the visual display includes an activatable getter for final evacuation of the display. Conveniently, this is positioned in the emission-device/peripheral-carrier-wall gap.

30

 According to a third aspect of the invention there is provided a method in the manufacture a field effect emission device of the first aspect of the invention, the method consisting in the steps of:

- forming an array of via apertures in a substrate;

- filling the via apertures with conductive material to form vias; and
- forming on one face of the substrate a series of conductive connection lines for emitters of an emission layer to be produced on the said face of the substrate, the emission layer to have:
 - 5 • a multiplicity of emitters and gates, arranged as an array of emission pixels;
 - the vias and at least some of the conductive connections being so positioned as to interconnect.

10 In one alternative, the forming of the emitter lines and the gate lines on the substrate fills the respective via apertures with conductive material of the said lines. Then, preferably, electrical connection tracks are formed on the face of the substrate opposite from the emission layer, with the tracks being so positioned as to interconnect with respective vias, the formation of the tracks connecting them with
15 the vias and the respective emitter and gate lines.

 Alternatively, electrical connection tracks can be formed first on the face of the substrate opposite from the emission layer, the tracks being so positioned as to interconnect with respective vias, with the formation of the tracks filling the via
20 apertures. The emitter and gate lines are then subsequently formed and connected by the vias so formed to the respective electrical connection tracks.

 Whilst it is envisaged that the lattice of conductive emitter and gates lines may be placed on the ceramic substrate by sputtering or like method, preferably the
25 electrical connection tracks and/or the emitter and gate lines are formed by screen printing; the substrate is formed by tape casting of ceramic material; and the via apertures are formed by stamping them in the tape cast ceramic material when in the green state. As an alternative to stamping, the substrate may be pierced by etching.

30 In one particular embodiment, the emitter lines in the case of the front substrate layer or electrical connection tracks in the case of other substrate layers are formed by screen printing onto a smooth release layer, the substrate is formed by tape casting ceramic material over the emitter lines, the via apertures are formed by

stamping and filled by screen printing. This latter will normal include printing of electrical connection tracks for the other side of the substrate layer, but can include screen printing into via apertures only.

- 5 Preferably the substrate is compressed between platens to cause the electrical connection tracks to be flush with the surface of the ceramic substrate.

- 10 Where the substrate has one or more additional layers with vias and electrical connection tracks formed in like manner, the layers are preferably compressed
together to form electrical contacts at interlayer interfaces before firing, preferably
having first been individually flattened by compression. 7

Preferably, the top surface of the substrate is polished in preparation for deposition of emitters on the surface.

15

- 7 In one embodiment, after screen printing of the emitter lines with the emission
layer in a "green state", it is compressed between platens to press the emitter line
stripes into the substrate. Next, the dielectric layer and the resistive layer - when
provided - are added. Preferably these are spun on. Then the gate lines are screen
20 printed on. The substrate has more than one layer and the layers are compressed
together to form electrical contacts at interlayer interfaces before firing, preferably
having first been individually flattened by compression. The compression together
ensures electrical contact at the vias. The assembly is then fired at elevated
temperature to sinter the materials of the substrate and the electrical components.
25 After firing, the gates and dielectric layer openings are made by micro-machining.
Then the emitters are electrolytically deposited and micro-machined.

- 30 According to a fourth aspect of the invention there is provided a substrate for a
field effect emission device produced by the method of the third aspect of the
invention.

Drawings of the Preferred Embodiments of the Invention

To help understanding of the invention, specific embodiments of it will now be described by way of example and with reference to the accompanying drawings, in which:

Figure 1 is a perspective view of a part of an emission device of the invention;

5 Figure 2 is a scrap cross-sectional view on a larger scale through the device of Figure 1, with a further enlarged detail;

Figure 3 is a perspective view of a stamped and apertured substrate, ready for screen printing of the emitter stripes;

10 Figure 4 is a scrap view on a larger scale of the piece of Figure 3 after screen printing of the emitter stripes;

Figure 5 is a similar view of the piece after screen printing of the gate lines;

Figure 6 is side view of the plurality of substrate pieces assembled for firing;

Figure 7 is a scrap side view of another substrate and electrical connection track lay up method;

15 Figure 8 is a view similar to Figure 5 showing a photo-resist layer for controlling etching of the gates;

Figure 9 is a perspective view of a second emission device of the invention;

Figure 10 is a scrap plan view of the back surface of the second emission device;

20 Figure 11 is a view similar to Figure 9 of a third emission device of the invention;

Figure 12 is a scrap view similar to Figure 9 from the back of the third emission device of the invention, showing in particular vias and conductive tracks, with the substrate layers not shown as such;

25 Figure 13 is a diagrammatic plan view of the layout of vias in the front substrate layer and respective driver chips on the back face for the emission device of Figure 11;

Figure 14 is a perspective view of a visual display unit of the invention before fitting of its face plate;

30 Figure 15 is a scrap cross-sectional view on a larger scale of part of the device of Figure 9 with its face plate fitted, with a further enlarged detail showing an inner spacer;

Figure 16 is a broken away scrap perspective view of an outer spacer on the face plate of the visual display unit of Figure 14;

Figure 17 is a view similar to Figure 14 of a larger visual display unit of the invention, without its face plate being shown;

Figure 18 is an underside view of the visual display unit of Figure 17;

Figure 19 is a view similar to Figure 15, showing an arrangement for
5 positioning emission devices on their carrier;

Figure 20 is a plan view of a corner of another visual display of the invention, showing an alternative arrangement for positioning emission devices on their carrier;

Figure 21 is a view similar to Figure 19 showing the alternative positioning arrangement of Figure 20;

10 Figure 22 is a scrap cross-sectional side view of a single substrate layer visual display of the invention;

Figure 23 is a similar view of a double substrate layer visual display of the invention;

Figure 24 is a block diagram of assembly apparatus according to the invention;

15 Figure 25 is a cross-sectional side view of an assembly station with a face plate shown only in outline;

Figure 26 is a partial plan view of the assembly station without a face plate;

Figure 27 is a cross-sectional side view of a sealing chamber;

Figure 28 is a view similar to Figure 15 showing an evaporatable getter
20 according to the invention;

Figure 29 is a scrap plan view of a corner of a visual display unit showing another, deformable getter according to the invention;

Figure 30 is a cross-sectional side view of a visual display unit of the invention, complete with driver chips;

25 Figure 31 is a perspective view of a emission device set up for cleaning by a similar device;

Figure 32 is a perspective view of a second embodiment of a sealing machine of the invention;

Figure 33 is a plan view of the machine of Figure 32;

30 Figure 34 is a front view of the machine of Figure 32;

Figure 35 is a view similar to Figure 32 of this machine configured differently;

and

Figure 36 is a similar view of a third sealing machine of the invention.

Description of a First Embodiment of the Emission Device

Referring to Figures 1 and 2, there is shown a representative part of a field effect emission device 100 for a visual display having a ceramic substrate 1. For compatibility with other components of the visual display, in particular a glass face plate (see below), the ceramic used for the substrate is alumina. On an emission side 2 of the substrate, it has an emission layer 3 including a lattice of conductive emitter and gates line stripes 4,5. In use, on a driver side 6 of the substrate, it has drivers 7 mounted and connected, as will be described in more detail below, see Figure 30. Provision of the drivers so close to the emission layer which they are driving
10 minimises capacitative and other electrical losses.

The emitter stripes are of nickel and the gate stripes are of chromium. The respective stripes of the same type are spaced across the substrate. They are separated at their intersections by a dielectric layer 8 and a thinner resistive layer 9 on the
15 substrate side of the dielectric layer. The dielectric layer is of silicon dioxide. The resistive layer can be of polycrystalline silicon or metal oxide. The emitter stripes are recessed into the surface of the emission side of the substrate, whereby the dielectric and resistive layers are planar. Typically, the stripes are arranged at a pitch of 80 per inch, i.e. at 0.0125" centres. Each stripe is 0.004" wide and 0.0004" thick.

20

At each intersection, an emission pixel 10 is provided. Each emission pixel has an array of emitters 11 and gates 12. The gates are openings 13 in the gate stripe 5 at the intersection, with aligned openings 14 in the dielectric layer 8. The emitters are elements 15 deposited on the resistive layer 9 over the emitter stripe 4 at the
25 intersection, in the openings 13,14 in the gate stripe and the dielectric layer. Typically 300 emitters are provided per pixel.

For electrical connection to the emitter and gate stripes, the substrate has apertures 16, into which the strip material – or other conductive material, see below –
30 extends as vias 17. The gate vias extend through the dielectric and resistive layers as well as the substrate.

To facilitate soldered, electrical connection to driver chips 7 (see below) connected to the back face of the device at contact pads 18, the device substrate is

made up of several substrate layers 1₁, 1₂, 1₃, 1₄ bonded together. Each layer piece has connection strips 19 set into its opposite surfaces and interconnecting vias 20, of the same material as the strips. The connection strips of adjacent layers abut or at least vias of one layer abut with connection strips of the next layer, providing electrical contact. The connection strips and the vias are arranged to spread or fan out the connections from the stripe pitch, typically 0.0125", to that of driver chip contacts, typically 0.050", to be connected to the contact pads 18. Where more lines to the inch are used, the stripe pitch will decrease, requiring more pronounced fan out.

10 Peripherally, the back/driver surface of the outer substrate layer 1₄ has an electrically isolated, screen printed, continuous metallic strip 21 - similar to the pads 18 - for sealing connection of the device to a carrier, described in more detail below. Power and signal supply tracks 22 are also provided on the back surface for powering the drivers and providing control signals to them.

15

 The emission device has edge zones 23, along the four edges of the ceramic substrate, into which the emitter and gate lines do not extend. Spaced along two opposite edge zones, the emission device has red, blue and green colour lines drive contacts 64_R, 64_B, 64_G on its emission side. These contacts are printed on top of the dielectric layer and connected by vias and connection strips to driver contact pads on the back surface of the substrate.

Each layer is of the order of 0.010" to 0.020" thick.

25 Manufacture of the above emission device will now be described. Other embodiments of emission device will be described below.

Description of the Preferred Method of Manufacture of the Emission Device

The emission device of Figure 1 is manufactured as follows:

30 The individual layer pieces 1₁, 1₂, 1₃, 1₄ of the alumina substrate 1 are formed by tape casting. The pieces are stamped from the tape cast material and have apertures 16 for the vias 17 cut in by photo-resist etching of fired ceramic or punching of the material in its green state. The array of via apertures shown in Figure 3, is illustrative only. Every emitter line and every gate line must have at least one via and

preferably two. The arrangement shown in Figure 3 has all the gate vias aligned and all the emitter vias aligned. Whilst this is convenient for logical layout, it causes lines of weakness. An improved layout is described below. Further it is convenient to form the emitter via apertures first.

5

7 Whilst the pieces are still green, the emitter stripes are screen printed as a powdered metal slurry onto the top one 1₁ of the pieces. Similarly connection strips 19 are screen printed on the other pieces 1₂, 1₃, 1₄. The screen printed material passes into the apertures to form the vias 20, the emitter stripe material filling the emitter via apertures and the connection strip material, which is typically silver based, filling the interconnection via apertures. The pieces are then individually compressed between platens to press the emitter stripes 4 and the connection strips 19 into the surfaces of the respective substrate pieces, see Figure 4.

15

Next, the dielectric and resistive layers 8,9 are added to the top one 1₁ of the pieces by spinning. The resistive layer is required only at the intersections of the emitter stripes and the gate stripes and can be etched away elsewhere before dielectric layer is added. Via apertures (not shown) for the gate stripes 5 are formed and the stripes are printed on and through the apertures, see Figure 5. All the layer pieces making up the substrate are then stacked and pressed together to ensure contact between respective connection strips and vias in adjacent layers. The assembly is fired, see Figure 6.

20

As an alternative to screen printing the conductive layers onto the green substrate, the conductive tracks 35, at for one side of a substrate layer 36, can be screen printed onto a release film 37, supported by a flat surface 38, as shown in Figure 7. The substrate material 36 is then tape cast over the conductive tracks, whereby a smooth level surface is achieved across the boundaries of the materials. The release material, which is shown in Figure 7 with exaggerated thickness, is peeled off when the tape casting has set, for subsequent operations, including via formation and substrate build up. With this method, the vias will require to be filled as a separate operation from laying down of the conductive tracks onto green substrate. This alternative method is applicable also to emitter lines laid onto a release film and overlaid with tape cast ceramic. The resistive layer also may be laid by screen

30

printing – first – preferably in the pattern described above, that it is only at the intersections between the emitter and gate line stripes. After build up of the substrate and its firing, the top layer is preferably polished to provide as even surface onto which the emitters are deposited, so that they are consistent and level with each other.

5

After firing, the gates and voids are made by micro-machining. Then the emitters are electrolytically deposited and micro-machined. This is achieved by depositing a photo-resist layer 31, see Figure 8, on the emission side of the substrate, selectively exposing and developing it, etching openings 32 in it where the gate
10 openings are to be formed. A separate etching process forms the gate openings 13. A further etching process forms the openings 14 in the dielectric layer down to the resistive layer 9. Not only is this electrically resistive, but also it is resistant to further etching.

15

Once the etching is complete, the emitters 11 are formed by building nickel onto the resistive layer where it is exposed at the bottom of the openings 14 in the dielectric. This can be either by vacuum deposition or by electro-deposition. The man skilled in the art will perform this process without the need for further description here.

20

Description of a Further Embodiments of the Emission Device

Referring now to Figures 9 & 10, the simplest form of emission device of the invention is there shown. It has a single ceramic layer. On its emission side is provided an emission layer 503 similar to the emission layer 3. As such it requires no
25 further description. This device suffers from the disadvantage that the fan out of conductive tracks 519 on the back side of the substrate layer 501, from vias 516 to contact pads 518 requires a tortuous layout of the tracks, bearing in mind that power and signal tracks 530 must also be provided to the driver chips 507 and that in Figure 10 the pitch of the vias has been shown as half that of the driver chip pins, whereas in
30 practice, the via pitch is likely to be smaller still by comparison. It should be noted also that whilst Figure 10 shows an ideal line 1 to pin 1 ... line n to pin n fan out, in reality the order of the pins is likely to cause a more complex layout to be necessary.

cl 12
cl 8 { Further, bearing in mind that the device must be pressure tight, in order to maintain the internal vacuum, the device suffers from the disadvantage of relying on complete

filling of the apertures for pressure integrity. Nevertheless it is anticipated that there may be applications for this simplest form of the emission device of the invention.

Referring now to Figures 11, 12 & 13, the emission device there shown has

5 two ceramic layers 6011, 6012. The back face 606 of the first layer has interconnection tracks 6191 extending from emitter line (for instance) vias 616 in the front substrate layer 6011, see Figure 12. It should be noted that in Figure 12, the individual layers as such are not shown; but the layout of the tracks on them is shown. The front face 6022 of the second layer 6012 also has interconnection tracks 6192, the

10 two sets tracks 6191, 6192 interconnect where they abut. The tracks 6191 fan out the pitch of the vias 616 to the pitch of the interconnection points 6030 by a factor of two. The tracks 6192 fan out again by being of sequentially longer length so that their ends are again at doubled pitch. Alternate ones of these ends have a via 6020 to tracks 6194 to chip pads 6181. Since it is alternate tracks which have vias at their ends, the

15 via pitch is again doubled, i.e. it is fanned out by a factor of eight from the pitch of the vias 616 in the front layer. The alternate tracks 6192 not having vias 6020 are continued transversely to further vias 60201 on the other side of the chip 607, with back surface tracks leading back to pads 6182 on the other side of the chip. Power and signal lines 630 also lead to the chip. It will be appreciated that the two substrate

20 layers gives far greater flexibility in fan out than is possible with one layer, in that the tracks 6191, 6192, 6193 could if need be cross the power and signal tracks 630 to the driver chip 607. Alternatively, power and signal tracks can be more flexibly laid out in that they can pass by vias to the layer interface so that their relative order can be reorganised for instance. Further the vias 616, 6020 in both ceramic layers are

25 blanked off by piece of the ceramic substrate of the other layer, with the vias not being co-axial. This provides greater assurance of vacuum tightness.

*vias offset
cl 15*

In this embodiment, as shown in Figure 13 which is strictly diagrammatic, the vias, at least to the emitter and gate stripes are spaced in an array of aligned series of

30 vias in two alternate – in fact equal and opposite – orientations α, β to for instance the emitter line orientation A. Within the array, all the series are parallel to one or other of the orientations α, β . In one band across the substrate in the direction A, there are four aligned via series 616₁, 616₂, 616₃, 616₄. These represent two series 616₁, 616₂ of

emitter vias and two series 616₃, 616₄ of gate vias. Within each series, successive vias are to successive emitter or gate lines, and a relatively small number of vias are arranged in each series, say 25, which represents ¼" (transversely of direction A, the actual length trigonometrically depending on the orientation α to the direction A) in a 100 line per inch display. Providing such a short series localises the weakening of the substrate layer introduced by the vias. From one of the series 616₁, the next of the series 616₂, i.e. the vias for the next 25 lines, is spaced by a gap 6166 from the previous one and set at the other orientation β . This introduces a transverse line of weakness. Provision of the gaps ensures that the overall weakness is minimised. The array is in effect a zig zag array with gaps 6166 between the zigs and the zags and an orientation γ of the aligned series. It will be noted that the arrangement, shown in Figure 13, spreads the via series horizontally of the Figure at twice the pitch as vertically. Thus the series 616₁, 616₂ will cross the emission device horizontally whilst reaching only half its height. Thus to make contact with all the emitter lines, it must be restarted again half way down the device. If the array of series is closed up horizontally, it is possible to avoid restarting. A particular configuration of the array which may be used is one in which the orientations β & γ are both equal to 45°. In this case, the series 616₂ are all not only parallel but themselves aligned. However weakness is avoided by the gaps. Further, to provide two vias per line, the array of series can be started again, with the starting point spaced horizontally as opposed to vertically as discussed above.

The series 616₃, 616₄ is for gate lines. Although these lines run transversely to the emitter lines, there are the same number and they are at the same spacing all over the emission layer. Thus their vias are set in a precisely similar pattern.

With each series of vias in the front face, a chip 607 is associated on the back face, conveniently in one for one correspondence. However one chip may service two series of vias or vice versa. As shown in Figure 13, all the chips are set to the same side of the vias. However, it will be appreciated that where the vias are close to an edge of the emission device, it is convenient to place the chips in board of the vias. Further, where driver chips having hundreds of driver output connections, in a rectangular array, are provided, the chip to via series relationship will not be one to

one and the fan out will be considerably more complex than that shown in Figure 12, but essentially within the ability of the man skilled in the art.

Description of the Preferred Embodiment of Visual Display

5 The visual display shown in Figures 14 & 15 includes the emission device 100 of Figures 1 to 6 and a carrier 40. This is tape cast of alumina material. It has a L-shape cross-section, comprising a foot flange 41 and an upstanding wall or web 42. These are separately tape cast and assembled together prior to firing. Four lengths 43,44,45,46, corresponding to the four sides of the carrier at the four sides of the
10 emission device 100, are arranged with butt joints at the corner. The flanges 41 have a continuous metallic track 47, complementary to the continuous metallic strip 21, screen printed and pressed into the surface of the ceramic on prior to firing. Similarly there are provided contacts 48 on the flange complementary to the supply tracks 22. The material of the contacts is continued onto the inwards facing surfaces 49 of the
15 carrier for providing electrical contacts as described in more detail below.

Anode Plate 51
20 As described below, the emission device 100 is soldered into the carrier 40. A sealing wall 50 of glass frit is provided around the top of the web 42. A glass front face plate 51 is mounted on the sealing wall at a predetermined spacing from the emission layer of the emission device. The inside surface of the face plate has phosphor material 52 printed on it for selective excitation by the emission device pixels.

25 The final components to be added to the visual display after the front plate is sealed are the drivers 7 (see Figure 30). These are soldered to the contact pads 18. At the same time a connector (not shown) is soldered to the contacts 48.

30 Turning now to Figure 16, the visual display, of which a portion is there shown, is a colour display. The phosphor material is provided as red, blue and green spots 52_R, 52_B, 52_G. One of each spot is provided opposite each emission pixel, whereby that pixel can display a selected colour. The spots are arranged in a uniform array across the face plate, with red, blue and green voltage lines 53_R, 53_B, 53_G interconnecting respective coloured spots across the face plate. The lines terminate at outer spacers 54 arranged at opposite sides of the display. The outer spacers are of

alumina ceramic, and are formed of two layers 55,56, with a via and connection track arrangement enabling contact ends 57_R,57_B,57_G of all of the lines of respective colours to be collectively connected to a respective common one of three contacts 58_R,58_B,58_G. The upper layer 55, which is laser tacked at its ends to the face plate 51, has red, blue and green vias 59_R,59_B,59_G leading to red, blue and green contacts 60_R,60_B,60_G on its side in contact with the glass. The contacts 60 abut the respective contact ends 57. The vias of the respective colours are staggered across the width of the spacer layer 55, and lead through to red, blue and green contact strips 61_R,61_B,61_G. Similarly the lower spacer layer 56 has red, blue and green contact strips 62_R,62_B,62_G running the length of its side abutted with the upper spacer layer, whereby each red, blue and green voltage lines 53_R,53_B,53_G is connected to the respective red, blue and green contact strips 62_R,62_B,62_G. The lower spacer layer 56 also has red, blue and green contact vias 63_R,63_B,63_G connecting the strips 62 to red, blue and green contacts 58_R,58_B,58_G on the side of the outer spacer 54 opposite from the face plate. The contacts 58 are large and largely spaced apart in comparison with the inter-phosphor line spacing to enable the face plate's positioning with respect to the emission device to be made with a tolerance greater than the said line spacing. The emission device has complementary contacts 64_R,64_B,64_G in its emission layer as described above.

Reverting to Figure 15, the visual display has a number of inner spacers 81 across its width, one only being shown. The spacer is for support of the face plate 51 and the ceramic substrate 1 against atmospheric pressure urging them towards each other. It is of tape cast ceramic, but could be of extruded glass. Typically it will be 0.002" thick and 0.050" high. It is set in a groove 82 in polyimide material in a phosphor layer 83. The polyimide is apertured to give the emitted electrons access to the phosphor spots 52 and covered with a reflective chromium layer in the manner conventionally used in a cathode ray tube. The inner spacers are initially adhered to the face plate 51, before this is assembled to the emission device as described below. The emission layer 3, in particular the gate stripe material 5, is also provided with a groove 84 for the opposite edge of the inner spacer, the spacer 81 registering with the groove 84 on assembly. The grooves are formed at masks (not shown) in the build-up of the surrounding material. As shown the spacer has a conductive line 85 running along it. The line is connected to a contact pad (not shown) for application of a voltage to divert electron emission from the spacer. Whilst the spacer shown in

Figure 15 is of rectangular cross-section, it may be tapered towards the face plate to minimise its effect in the visual display. Further, it may not extend across the full width of the display. It is envisaged that cruciform inner spacers, extruded from glass, may be used in place of straight spacers, with the arms of the cross extending in line with the pixel array between the emitters in both directions. The cruciform shape may taper towards the face plate. Such spacers 91 set out in an elliptical pattern 92 are shown in Figure 17. The pattern provides support over the entire area of the multiple emission device display there shown. Linear inner spacers 93 are also shown as an alternative in another portion of the display.

Description of Further Embodiments of the Visual Display

Turning now to Figure 17 & 18, the display there shown is similar to that shown in Figures 14, 15 & 16, except that it is larger. The emission devices 71 included in it can be made only to certain dimensions, usually 4" square. To make the display larger, it has a plurality of emission devices abutted edge to edge. As shown, the display has four emission devices 71, giving it an 8" square size.

The emission devices 71 are identical with the emission devices 1, except that along two side edges 72, the edge zones are not present and the emitter and gate line arrays extend to the very edge of the ceramic substrate. One advantage of using alumina as a ceramic material of the substrates is that it can be cut, microdiced, to accurate tolerances. Thus the edges can be cut to be one half the pixel pitch from the emitter or gate line adjacent to the edge. The arrangement is such that where two emission devices are abutted edge-to-edge, the array of emission pixels is continuous from one device to the next. The other edges 75 of the emission devices can be machined to closely fit the side walls 42 of the carrier, along their length as shown in Figure 19, to give positive alignment of the devices in the carrier. Alternatively, the edges 75 can be cut away between location projections 76, conveniently at the corners of the emission devices, as shown in Figures 20 & 21. This provides a channel 77 for a getter 301, such as described in more detail below. The channel is recessed into the carrier to accommodate a deep getter. As an alternative to the projections on the corners of the tiles, the carrier can be provided with location lugs 761 in the channel 77, which perform the same function. It should be noted that the front plates 51 of the displays shown in Figures 19, 20 & 21 extend laterally beyond the carriers 40. This

facilitates connection to the phosphor lines when connection is not made through spacers and edge connectors (not shown) are used. The lateral extension also provides a rim which can be gripped for manipulation prior to sealing as described in more detail below. In Figure 21, an alternative for phosphor line connection is
5 provided in the form of connection tracks 78 on the outside of the carrier. They pass onto the top of the carrier, where contact is made with the phosphor lines via conductive frit 79.

To support the joints between two devices, the carrier is provided with
10 additional flange pieces 73 bridging the side members of the carrier behind the joints in the devices. Thus in the four emission device display shown, the carrier forms a square surround with an internal cross. The emission devices are soldered to the cross piece 73 in the same way as to the flanges 41, that is to say with a high temperature solder joining strips around the back face of the devices to tracks 47 along the carrier
15 members. The solder can be a brass or an indium based solder. Where the adjacent emission devices require to be interconnected for their synchronisation, contacts 481 on the carrier's bridging members and complementary contacts (not shown) on the emission devices are provided. They are joined in the high temperature soldering process. In order to provide room for the contacts 481 between the solder
20 tracks 47, the latter and the bridging members 73 are locally widened, with the contacts 481 provided between the tracks.

Turning now to Figure 22, a simpler form of visual display of the invention is shown where the face plate 511 is connected to the single substrate layer emission
25 device 501, of Figures 9 & 10, by means of a thick, glass frit strip 510, without the interposition of any wall. The phosphor lines 531 are not taken to the substrate, but pass straight out sideways for connection to drivers (not shown).

Figure 23 shows another simple display, this having two substrate layers.
30 Again the face plate 511 and the substrate 6011, 6012 are joined without the interposition of a carrier. A glass wall 421 is attached between the two and adhered to them by ultra-violet light curing adhesive 4211, on both sides. The adhesive is cured at both sides of the wall by a single irradiation of UV light. To provide additional

structural strength, the emission device is adhesively secured to a plastics material carrier 411 at the back of the device.

Description of a First Embodiment of Assembly Apparatus of the Invention

5 Referring to Figures 24 to 26, the assembly apparatus there diagrammatically shown has an assembly station 201 with a number of ancillary stations associated with it, in particular an emission device cleaning station 202, a sub-assembly pre-heating station 203, a face plate cleaning station 204, a face plate pre-heating station 205 and an evacuation unit 206. Components are moved between the stations by means whose
10 design is within the ability of the man skilled in the art and will not be described here.

The emission device cleaning station 202 incorporates a cleaning emission device 101, as described below, set up for cleaning emission devices 1 to be assembled. The sub-assembly pre-heating station 203 incorporates heaters (not
15 shown) for heating a sub-assembly of however many - four as shown in Figure 26 - of the emission devices 1 on their carrier 40 as will be assembled into a visual display. The face plate cleaning station 204 has another such cleaning emission device 101 similarly set up for cleaning face plates 51 to be assembled. The emission device pre-heating station 205 incorporates heaters (not shown) for heating the face plate 51 to be
20 assembled into the visual display. The evacuation unit 206 comprises a roughing pump 207 and a high vacuum pump 208 in series. The assembly station 201 includes a vacuum chamber 209, in which the assembly is carried out. Vacuum lock valves 210 through which components can be passed whilst maintaining a vacuum in the chamber 209 are provided.

25

Within the chamber 209, there is a datum jig 211 for locating the carrier 40, on introduction of a sub-assembly through the valve 210 from its pre-heating station 203. Below the jig are positioned radiant heating elements 212 aligned with the carrier's flanges 41,73 for heating them to the temperature at which solder between them and
30 the ceramic substrates 1 melts.

Over the jig 211 is arranged at least one optical position sensor 213 and a plurality of robotic arms 214, for manoeuvring the substrates 1 on their carrier to their design position. Once positioned, they are temporarily secured by aluminium wedges

215, which were included with the sub-assembly and which are pressed into position by the robotic arms. The same robotic arms are adapted for manoeuvring the face plate 51 (shown in outline in Figure 25) into position on the positioned sub-assembly.

5 Adjacent the radiant heating elements 212 are ducts 216 leading to the vacuum unit for drawing air flow past the flanges 41,73 for cooling of the solder once the emission devices have been positioned and wedged.

10 Within the chamber 209, also mounted over the jig 211, is provided a tacking laser 217 on a track 218 allowing it to be moved into alignment with various points on the periphery of the carrier for tacking of the face plate 51 to the glass frit 50 on the wall 42 of the carrier.

Description of the Preferred Method of Cleaning the Emission Device

15 In Figure 31 is shown the emission device of Figure 1 arranged opposite another similar device 101, having its drivers 107 controlled to provide a maximum electron beam irradiation of the emission layer 3 of the device 100. The devices are set up close to each other, preferably but not necessarily in a vacuum chamber. They are sufficiently close for the electron irradiation from the device 101 to activate and
20 displace any molecular debris on the emission device which cannot be removed by conventional washing techniques.

 The emission device 101 is powered for a length of time sufficient for cleaning of the device 100.

25

Description of the Assembly Method using the First Assembly Apparatus

 Turning again to Figures 24 to 26, a sub-assembly of four emission devices 1 on a carrier 40 is introduced into the emission device cleaning station 202, where the devices are electronically cleaned as described above. The sub-assembly is then
30 moved on, on guides which are not shown, to the sub-assembly pre-heating station 203, where it is pre-heated. Again it is moved on to the assembly station 201. Simultaneously, a face plate is cleaned at face plate cleaning station 204 and pre-heated at the pre-heating station 205. The vacuum chamber 209 is pre-heated and evacuated to a substantial vacuum by means of the pumps 207,208.

The sub-assembly is introduced into the vacuum chamber via the vacuum lock 210 and positioned on the jig 211. Preliminarily to having been cleaned, high temperature solder, i.e. having a melting point of c.300°C, was screen printed onto strips 21 and tracks 22 of the substrates 1. The temperature in the pre-heat station is not hot enough to melt the solder, but the heating elements 212 heat the carrier and the substrates locally to melt the solder and cause it to flow and wet the complementary track 47 and contacts 48 on the carrier.

10 Whilst the solder is still molten, the robotic arms are manipulated to contact the free edges of the 220 of the emission devices. One optical sensor 213 is located centrally of the emission devices and can detect the joint lines 221 between the devices. The four joint lines between the four devices meet in a cross 222 of which the opposite limbs 223,224 align when the emission devices are correctly positioned
15 with respect to each other. The central sensor is associated with a light recognition system (not shown) such that it can control the robotic arms 214 to manipulate the emission devices into correct positioning. To ensure correct rotational positioning on the carrier, further sensors 213 are provided radially of the cross 222. Once the positioning is correct, the robotic arms are used to press the aluminium wedges 215
20 into position between the edges 220 and the walls 42 of the carrier - the wedges having been added to the sub-assembly prior to its cleaning.

 Immediately on wedging, the vacuum pumps are operated, to draw out the air introduced with the sub-assembly and the face plate which is now introduced. The
25 inlets to the pumps are the ducts 216 adjacent to the heating elements, whereby the cooling effect of the flow of withdrawn air is concentrated locally to the soldered joints which now solidify. This creates a hermetic seal peripherally of each emission device.

30 The face plate is introduced to rest via its spacers 54 on the emission devices. The respective contacts 63 and 64 align. A small gap 223 (see Figure 15) is present between the underside of the face plate at its edges and the frit 50 on top of the walls. Erasable, printed symbols (not shown) on the front of the face plate are viewed by the

sensors 213, and the robotic arms manipulate the face plate into pixel/pixel alignment with the emission devices. With the face plate held by the robotic arms, the laser 217 is activated to make tacks between the glass of the face plate and the frit 50. It should be noted that the frit has a trapezoidal cross-sectional shape, which causes it to form an upwardly curved meniscus when it is melted by the laser. This enables the joint between the frit and the face plate to jump the gap 223, which is of the order of 0.020" (0.5mm). Typically four tacks are made, one at each edge of the rectangular face plate. The latter is thus held in fixed position with respect to the carrier, to which the emission devices have been fixed on solidification of the solder.

10

Description of a First Embodiment of Sealing Apparatus of the Invention

Connected to the vacuum chamber 209 via one of its lock valves 210 is a second, high vacuum chamber 230 with a separate high vacuum pump 231. The chamber is equipped with a jig 232 similar to the jig 211 and a laser 233 and track 234 similar to the laser 217 and its track 218 in the first vacuum chamber 209.

15

Description of the Sealing Method using the First Sealing Apparatus

Referring to Figure 27, on introduction of the visual display into the sealing chamber 230 and its positioning on the jig 232, the pump 231 is operated to draw a high vacuum in the chamber. The laser 233 is aligned with the frit 50 at the periphery of the face plate, either at a preliminary tack or elsewhere. The laser is fired and traversed around the entire periphery of the face plate, welding it to the frit in the same manner as the tacks were made. Since the gap exists between the face plate and the frit prior to the welding, the evacuation can be continued simultaneously with the welding, with air being evacuated from the display via the gap. Completion of the traverse of the periphery completes the sealing.

20

25

Description of the Preferred Visual Display Evacuator of the Invention

Referring to Figure 28, the visual display of which a portion is there shown has an evaporatable getter 301 of barium. It is of foil twisted around quadrant pieces 302 of ceramic material spaced along the carrier 40. The getter is positioned in the space 303 between a spacer 54 and the carrier wall 42, whereby on evaporation of the getter by irradiation with a laser acting through a clear marginal piece 304 of the face

30

plate; the evaporated material deposits on the surfaces around the space, which do not include active parts of the emission layer nor of the face plate.

Figure 29 shows an alternative, non-evaporatable getter 311, extending a corner 312 of each emission device 100. The getter is formed as an invert C with the ends of the limbs between the edges 220 of the ceramic substrates and the walls 42 of the carrier. The arrangement is such that pressure on the upper part 313 of the getter section spreads it to cause it to act as a wedge during positioning of the emission devices.

10

Description of the Preferred Evacuation Method of the Invention

After sealing of the visual display with either an evaporatable or a non-evaporatable getter 301,311, the laser 234 is traversed to heat the getter to its active temperature at which it will absorb the majority of any gases still present in display after sealing. The activation of the getter can be immediately subsequent to the sealing whilst the display is still in the sealing chamber 230. Alternatively, it can be carried out later at room temperature.

The completed visual display is prepared for use by screen printing solder onto the contact pads 18 for soldering on of its driver chips 7.

20

Description of a Second Embodiment of Combined Assembly and Sealing Apparatus

Turning now to Figures 32 to 35, the apparatus there shown is for assembling face plates 753 to pre-assembled emission devices and carriers 754, referred to below as cathodes.

25

The emission devices and carriers are pre-assembled in a station – not shown – which heats them to melt the solder joining them and cools them to set the solder. Use of emission devices cut to fit their carrier avoids the need for manipulating them with respect to the carrier. Getter strips 301 are added to the channels 77, to complete pre-assembly of the cathodes.

30

The apparatus has three stations 701,702,703. The first 701 is a preheater, the second 702 is an alignment and irradiation station and the third 703 is a controlled

cooling station. A conveyor 704 is provided for feeding superimposed face plates and cathodes through a first gate valve 705 into the preheater. Thence, an internal conveyor operable by a knob 706 moves them through another gate valve 707 to the second station 702 and through a third gate valve 708 to the cooling station 703. It
5 has a final gate valve 709 through which sealed field effect emission devices are removed.

Beneath each station, a vacuum pump 710 capable of drawing ultra-low pressures is provided. Each station is isolatable from its pump by a gate valve 711.

10

The preheater is precisely that and is equipped with upper and lower banks of radiant heaters and reflectors 712. The upper heaters are provided above a quartz window 713 of a chamber 714 constituting the station. The lower heaters are provided within the chamber, that is above a bottom plate 715 of it which incorporates
15 an aperture to the station's gate valve and vacuum pump. The heaters heat the face plate and cathode to a temperature close to but lower than the melting point of the solder uniting the emission devices with the carrier. This temperature is not exceeded in the apparatus except locally on melting of the frit. The pressure in the preheater is pumped down to that in the alignment and irradiation station prior to
20 opening of the gate valve between them and transfer of the face plate and cathode, with the result that this second chamber is kept constantly evacuated.

At the alignment and irradiation station, further heaters 716 are provided. Those above the face plate and cathode, the face plate being uppermost, are mounted
25 on frames 717 about hinges 718, whereby they can be swung up to clear this station's top quartz window, exposing the face plate to the view of an optical system 719 and a laser 720. These are mounted on an X-Y stage 721 extending from the back of the apparatus.

30 The conveyor in this station 702 can be locked stationary, thereby locking the cathode stationary. Manipulation controls 722 are provided for manipulating the position of the face plate to be in pixel alignment, as measured by the optical system 719, with the cathode. The optical system is adapted to measure not only X-Y alignment, but also parallelism and Z separation. Once the X-Y alignment and the

parallelism is correct, the station is finally pumped to 10^{-8} Torr and the face plate is lowered to a controlled small separation from the frit on the carrier wall. The laser is traversed around the frit at close to full power to degas finally the frit. The laser is then traversed again at full power. The final traverse melts the frit which was already
5 close to its melting point. One traverse only at full power is adequate to cause the frit to rise by capillary action into contact with the face plate and freeze off once the laser has been traversed further. Continuous traverse of the frit provides that it is only local to the present position of the irradiation that the temperature of the frit is brought to its glass melting point. Elsewhere, the components are held cooler and below the
10 melting point of the high temperature solder. Localising the elevated temperature at the laser obviates substantial thermal stress build up and resultant cracking. A small overlap is provided at the end of the traverse. As soon as the frit has frozen off at the overlap, the laser's travel is changed to irradiate the portions of getter material provided in the channel in the carrier.

15

The cooling station 703 has meanwhile been pumped down and the sealed device is transferred to it. The temperature of the device is allowed to rise very slowly, in order to reduce the risk of thermal cracking to as great an extent as possible. As the temperature slowly falls, air is slowly introduced, so that the finished
20 device can be removed to the ambient surroundings.

Referring now to Figure 36, an alternative sealing apparatus is there shown, which is adapted to higher volume, automated processing. At the input end of the apparatus, a pair of pods 801,802 are provided, in which are respectively loaded
25 cassettes 803,804 of face plates and cathodes. The pods are provided internally with heaters 805 and vacuum pumps (not shown) The pods are connected to an input robot station 806, with a robotic arm 807. Two cleaning stations 808,809 are provided peripherally of the robot station 806. Each has its own vacuum pump 810. They are provided with electron and/or ion radiation sources 811,812, the former being an
30 emission device of the invention and the later being a source of inert gas plasma, for instance.

The robotic arm is adapted to unload the face plates and cathodes 813,814 from their pods for cleaning at the stations 808,809. Here a face plate is irradiated

under vacuum to degas the phosphor material in particular, to ensure that it does not release further gas in service. Similarly the cathodes are irradiated to remove molecules clinging to the tips of the emitters in particular. The cleaned devices are then loaded into a sealing station 815, essentially similar to station 702 of the previous
5 embodiment. Downstream of this is an output robot 816, adapted to take sealed displays from station 815 and load them into a cassette (not shown) in an output pod 817. This has temperature and pressure control for slowly returning the finished displays to ambient temperature.

10 The pods are detachable from the robots as their cassettes are emptied and refilled.

 The apparatus described is essentially modular, whereby the cleaning stations and the sealing stations can be duplicated as necessary to avoid the speed of the
15 slowest limiting the processing speed of the entire apparatus.

CLAIMS:

1. A field effect emission device for a visual display comprising:
 - a substrate and
 - an emission layer on one face of the substrate, the emission layer having:
 - 5 • a multiplicity of emitters and gates, arranged as an array of emission pixels
 and
 - conductive connections in the emission layer to the emitters and the gates;
 - the substrate having:
 - 10 • conductive vias provided through the substrate or at least a front layer
 thereof to at least some of the said conductive connections in the emission
 layer for electrical connection to their emitters and gates.
2. A field effect emission device as claimed in claim 1, wherein the conductive connections are emitter and gate lines to which the vias connect.
3. A field effect emission device as claimed in claim 2, the vias are positioned with
 - 15 emitters or gates positioned on the lines to both sides of the position of the vias.
4. A field effect emission device as claimed in claim 2 or claim 3, wherein each of the emitter and gate lines has a plurality of vias connected to it.
5. A field effect emission device as claimed in claim 1, claim 2, claim 3 or claim 4, wherein the substrate has a single layer, with electrical connection tracks and
 - 20 preferably driver contact pads provided on its face opposite from the emission layer.
6. A field effect emission device as claimed in claim 1, claim 2, claim 3 or claim 4, wherein the substrate has at least one substrate layer additional to the front substrate layer,
 - the or each said additional substrate layer having conductive vias
 - 25 therethrough,
 - electrical interconnection tracks being provided at the interface(s) between the
 or each adjacent pair of substrate layers for electrical interconnection of the
 vias of the pair(s) of adjacent layers and
 - electrical connection tracks and preferably driver contact pads being provided
 - 30 on an outer face of a back one of the additional substrate layer(s) opposite
 from the front substrate layer.

7. A field effect emission device as claimed in claim 6, including at least one intermediate, additional substrate layer between the front and the back substrate layers.
8. A field effect emission device as claimed in claim 6 or claim 7, wherein the said
5 electrical interconnection tracks provided at the interface(s) between the or each adjacent pair of substrate layers are provided on one only of the respective substrate layers at the interface(s), inter-layer contact being between vias of one layer and tracks of the other layer.
9. A field effect emission device as claimed in claim 6 or claim 7, wherein the said
10 electrical interconnection tracks provided at the interface(s) between the or each adjacent pair of substrate layers are provided on both of the respective substrate layers at the interface(s), inter-layer contact being between tracks of one layer and tracks of the other layer.
10. A field effect emission device as claimed in any one of claims 6 to 9, wherein no
15 gate line nor emitter line connection via is coincident, from the front substrate layer to the next, with a via in the next substrate layer.
11. A field effect emission device as claimed in any preceding claim, wherein the gate line and emitter line vias are arranged in at least the substrate layer having the emission layer in an array of aligned series of vias in two alternate orientations, both
20 orientations being offset with respect to the emitter and gate line directions, within the array, all the series are parallel to one or other of the orientations.
12. A field effect emission device as claimed in claim 11, wherein the array of aligned series of vias is a zig zag array with gaps between the zigs and the zags.
13. A field effect emission device as claimed in claim 12, wherein one of the alternate
25 orientations is equal to the orientation of the aligned series, and alternate series of vias are not only parallel but themselves aligned.
14. A field effect emission device as claimed in any preceding claim, wherein the vias are apertures in the substrate layers, which are filled with sintered metallic material.
15. A field effect emission device as claimed in any preceding claim, wherein the
30 substrate is of ceramic, preferably alumina.
16. A field effect emission device as claimed in any preceding claim, wherein at least some of the electrically conductive connections, lines, connection tracks and interconnection tracks are locally recessed into the material of the substrate layer(s).

17. A field effect emission device as claimed in any preceding claim, including drivers mounted on the back face of the back layer.
18. A field effect emission device as claimed in any preceding claim, wherein the substrate includes additional vias and conductive tracks for providing electric
5 connection through the substrate for phosphor excitation lines.
19. A field effect emission device as claimed in any preceding claim, wherein the back face of the substrate has a peripheral metallic stripe for solder connection of the device into the visual display.
20. A field effect emission device as claimed in any preceding claim, including power
10 and signal supply tracks on the back surface of the back layer for powering the drivers and providing control signals to them.
21. A field effect emission device as claimed in claim 2 or anyone of claims 15 to 20 as appendant thereto, including:
- a planar dielectric layer separating the emission lines and the gates lines and
 - 15 • a resistive layer on the emitter line side of the dielectric layer.
22. A field effect emission device as claimed in claim 2 or anyone of claim 15 to 21 as appendant thereto, wherein:
- the gates are circular apertures in the gate line stripes, and
 - the emitters are pointed features projecting towards the gate apertures through
20 voids in the dielectric layer.
23. A visual display comprising:
- a field emission device as claimed in any preceding claim;
 - a glass face plate incorporating phosphor material selectively excitable by the emission device pixels; and
 - 25 *25* • fused sealing material peripherally sealing the face plate to the emission device, whereby the face plate is parallelly spaced from the emission layer of the emission device and the space therebetween is evacuated.
24. A visual display as claimed in claim 23, including a carrier attached to the face of the emission device opposite from its emission layer.
- 30 25. A visual display as claimed in claim 23 or claim 24, wherein the sealing material is interposed directly between the face plate and the emission device.
26. A visual display as claimed in claim 23 or claim 24, wherein the sealing material is provided on a wall interposed between the face plate and the emission device.

27. A visual display as claimed in claim 24, wherein the fused sealing material is provided on a peripheral wall which is sealed to the carrier and extends from it to the face plate or which forms one limb of the carrier which is of L-shaped cross-section and extends towards the face plate, the face plate being sealed to the wall by the fused sealing material and the emission device being sealingly attached to the carrier at the face of the emission device opposite from its emission layer.
28. A visual display as claimed in claim 26 or claim 27, wherein the emission device is secured to the carrier by means of adhesive.
29. A visual display as claimed in claim 26 or claim 27, wherein the emission device is secured to the carrier by means of solder.
30. A visual display device as claimed in claim 29, wherein the solder is a high temperature solder, mating portions of the device and the carrier being provided with complementary metallic tracks, to one of which the solder was preliminarily applied.
31. A visual display device as claimed in claim 29 or claim 30, wherein the back layer of the ceramic substrate and the carrier include metallic tracks also connected by high temperature solder for electric power and drive signal connection to the device.
32. A visual display device as claimed in any one of claims 26 to 31, wherein the carrier is of the same material as the ceramic substrate and preferably of laminated construction.
33. A visual display device as claimed in any one of claims 28 to 31, wherein the carrier is of high temperature plastics material.
34. A visual display device as claimed in any one of claims 23 to 33, wherein the fused sealing material comprises fused glass frit.
35. A visual display device as claimed in claim 34, wherein the frit has sloping sides, preferably of trapezoidal cross-section.
36. A visual display device as claimed in any one of claims 23 to 35, including an array of spacers between the face plate and the emission device.
37. A visual display device as claimed in claim 36, wherein at least some of the spacers are provided within the area of the phosphor material and the emission layer.
38. A visual display device as claimed in claim 36 or claim 37, wherein at least some of the spacers are provided peripherally of the phosphor material on the face plate and the emission layer on the substrate.
39. A visual display device as claimed in claim 38, wherein one or more of the peripheral or outer spacers includes vias and/or contact tracks for the phosphor

excitation lines, whereby the phosphor pixels can be excited by drivers carried on the emission device.

40. A visual display device as claimed in claim 36 to 39, wherein one or more of the spacers within the area of the phosphor material and the emission layer, i.e. the inner
5 spacers, carries an electrical track for repelling emitted electrons.

41. A visual display device as claimed in claim 40, wherein the inner spacers are set in grooves in the ceramic substrate.

42. A visual display device as claimed in claim 40 or claim 41, wherein the inner spacers are short – laterally of the emission device – in lengths and/or crosses and are
10 preferably thin in comparison with the pixel line spacing and taper towards the face plate, whereby they do not interfere with any of the pixels and preferably have a tapered cross-section.

43. A visual display device as claimed in claim 27 or any of claims 30 to 42 as appendant to claim 27, wherein the emission device and the peripheral, carrier wall
15 are complementarily shaped, for locating the emission device on the carrier.

44. A visual display as claimed in claim 43, wherein the peripheral, carrier wall defines a space into which the emission device fits with negligible gap between the emission device and the wall.

45. A visual display as claimed in claim 43, wherein the peripheral, carrier wall
20 defines a space which is larger than the emission device, one of the wall and the emission device having projections for engaging with the other, for location of the emission device, a gap being present between the wall and the emission device between the projections.

46. A visual display device as claimed in claim 27 or any of claims 28 to 45 as
25 appendant to claim 27, wherein the device includes a plurality of emission devices and wherein the carrier has additional members bridging the side members of the carrier, the emission devices being in pixel alignment and supported and sealed at abutting edges by the bridging members.

47. A visual display as claimed in claim 46 as appendant to claim 43, claim 44 or
30 claim 45, wherein the emission devices are dimensioned at abutting edges for pixel alignment and at peripheral edges for abutment with the peripheral carrier wall.

48. A visual display as claimed in any one of claims 23 to 47, including an activatable getter for final evacuation of the display.

49. A visual display as claimed in claim 48 as appendant to claim 45 or to claim 46 as appendant to claim 45 or to claim 47 as appendant to claim 45, wherein the activatable getter is positioned in the emission-device/peripheral-carrier-wall gap.

50. A visual display device as claimed in any one of claims 46 to 49 as appendant to claim 29, claim 30 or claim 31, wherein bridging members and the emission devices are provided with complementary solder contacts for providing electrical contact between the circuitry of the adjacent emission devices.

51. A visual display device as claimed in any one of claims 23 to 49, wherein a respective red, green and blue phosphor spot is provided for each of emission pixel, whereby each pixel can be controlled to illuminate any or all three spots at will.

52. A method in the manufacture of a field effect emission device as claimed in any one of claims 1 to 22, the method consisting in the steps of:

- forming an array of via apertures in a substrate;
- filling the via apertures with conductive material to form vias; and
- forming on one face of the substrate a series of conductive connection lines for emitters of an emission layer to be produced on the said face of the substrate, the emission layer to have:
 - a multiplicity of emitters and gates, arranged as an array of emission pixels;
 - the vias and at least some of the conductive connections being so positioned as to interconnect.

53. A method as claimed in claim 52, wherein the forming of the emitter lines and the gate lines on the substrate fills the respective via apertures with conductive material of the said lines.

54. A method as claimed in claim 53, including the step of forming electrical connection tracks on the face of the substrate opposite from the emission layer, the tracks being so positioned as to interconnect with respective vias, the formation of the tracks connecting them with the vias and the respective emitter and gate lines.

55. A method as claimed in claim 54 as appendant to claim 52, including the step of forming electrical connection tracks on the face of the substrate opposite from the emission layer, the tracks being so positioned as to interconnect with respective vias, the formation of the tracks filling the via apertures, the emitter and gate lines being

subsequently formed and connected by the vias so formed to the respective electrical connection tracks.

56. A method as claimed in any one of claims 52 to 55, wherein the formation of the electrical connection tracks and/or the emitter and gate lines is by screen printing.

5 57. A method as claimed in any one of claims 52 to 56, wherein the formation of the substrate is by tape casting of ceramic material.

58. A method as claimed in claim 57, wherein the formation of the via apertures is by stamping them in the tape cast ceramic material when in the green state.

10 59. A method as claimed in claim 52, wherein the emitter lines in the case of the front substrate layer or electrical connection tracks in the case of other substrate layers are formed by screen printing onto a smooth release layer, the substrate is formed by tape casting ceramic material over the emitter lines, the via apertures are formed by stamping and filled by screen printing.

15 60. A method as claimed in claim 54 or claim 55 or any one of claims 56, 57 and 58 as appendant to either of claims 54 and 55 or claim 59, wherein the substrate is compressed between platens to cause the electrical connection tracks to be flush with the surface of the ceramic substrate.

61. A method as claimed in claim 60, wherein

- 20 • the substrate has one or more additional layers with vias and electrical connection tracks formed in like manner to those of claim 55, and
- the layers are compressed together to form electrical contacts at interlayer interfaces before firing, preferably having first been individually flattened by compression.

25 62. A method as claimed in any preceding claim, wherein the top surface of the substrate is polished in preparation for deposition of emitters on the surface.

63. A substrate produced by the method of any one of claims 52 to 61 for a field emission device as claimed in any one of claims 1 to 22.

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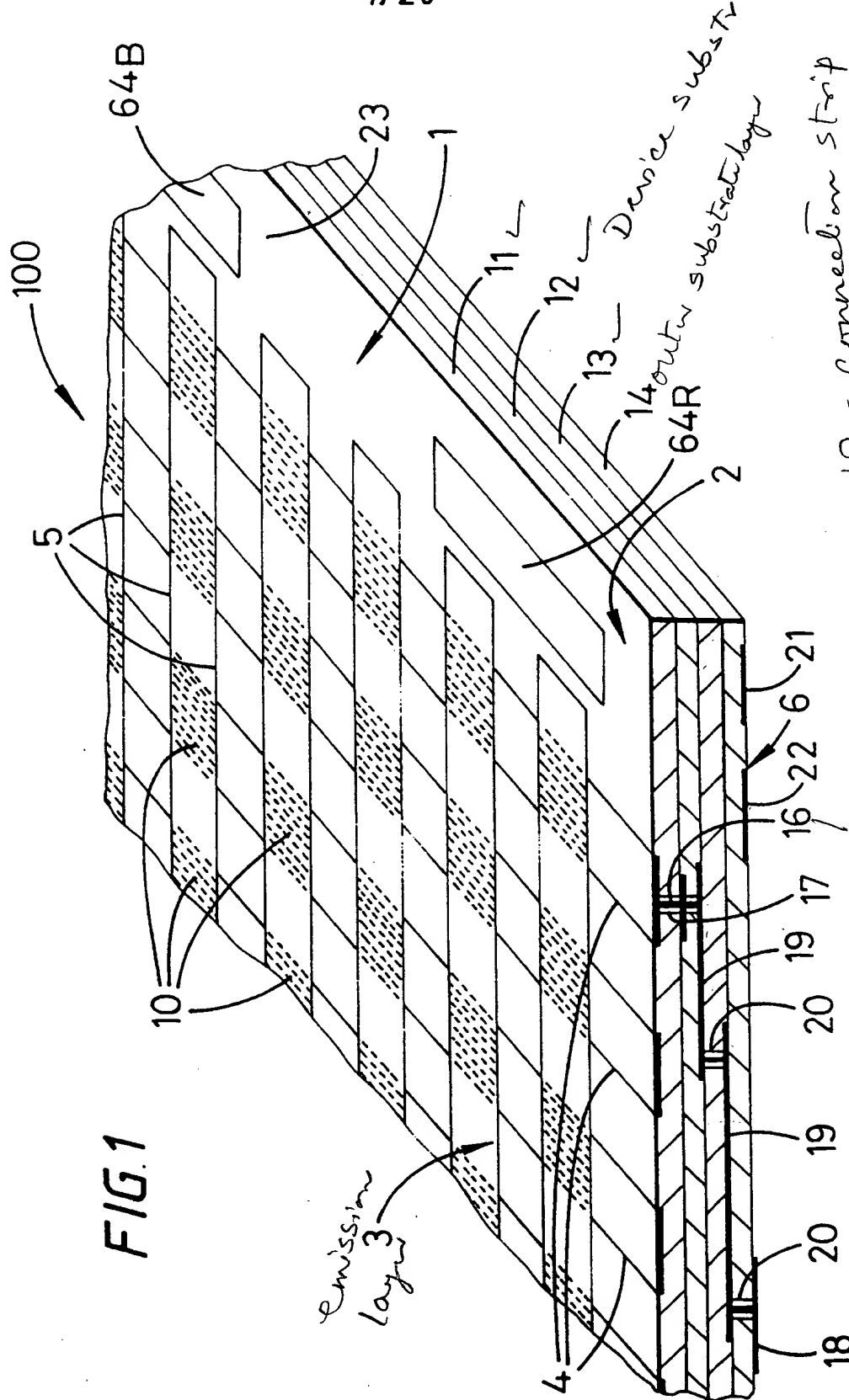


FIG. 1

Emission layer 3

contact pads

aperture

17 - via

19 = connection strip
20 - vias

cathode plate back layer front
back plate layer

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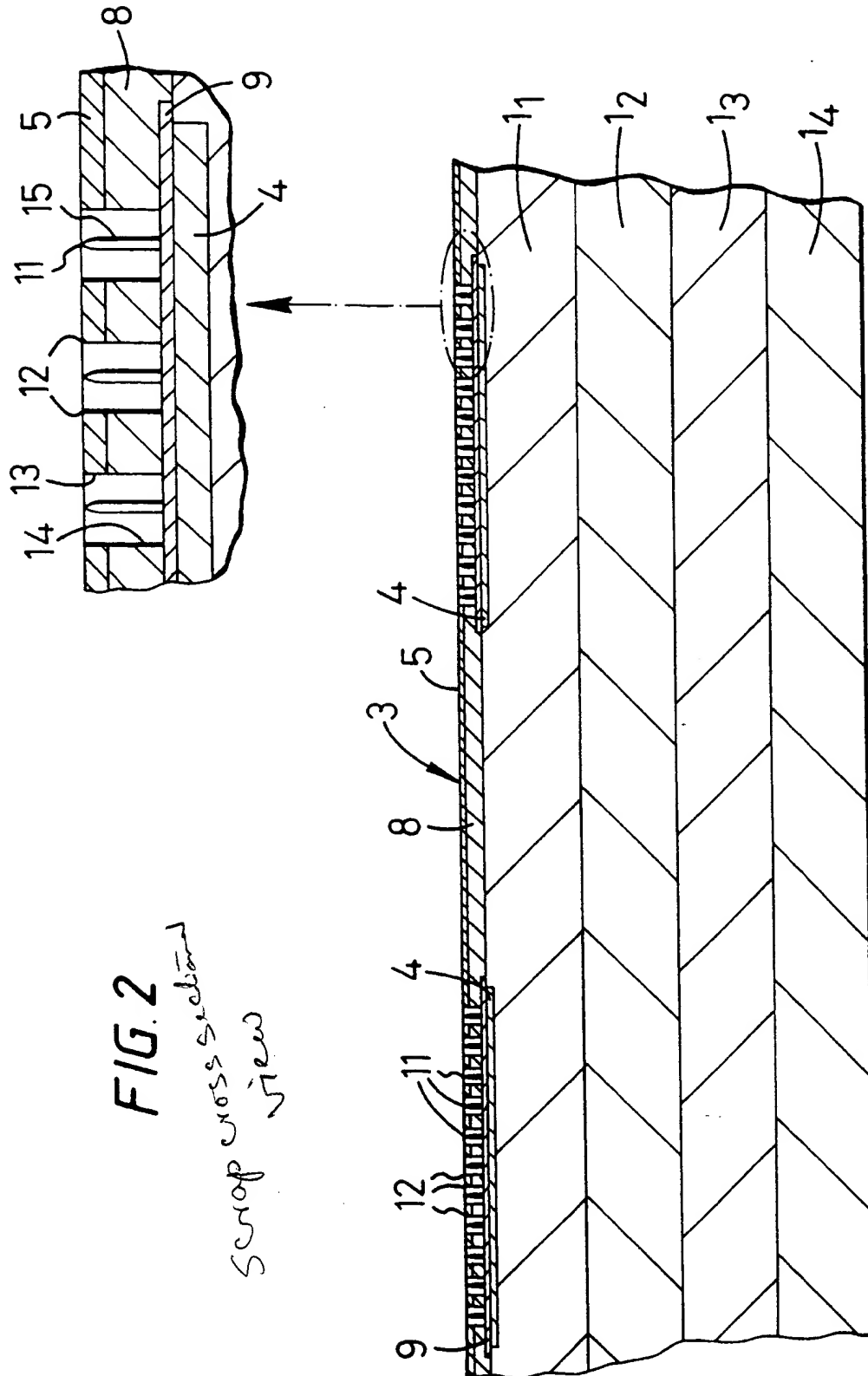


FIG. 2
Scrap cross-sectional
view

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FIG. 3

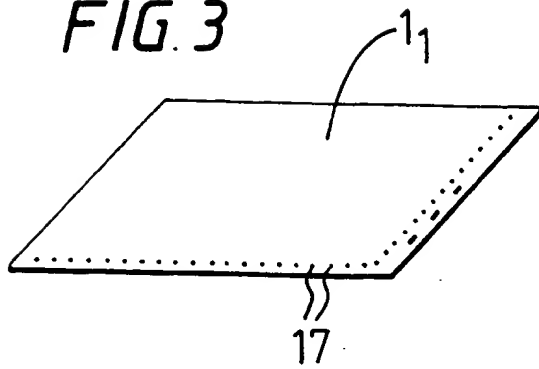


FIG. 4

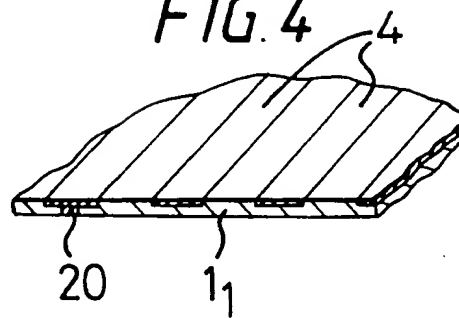


FIG. 5

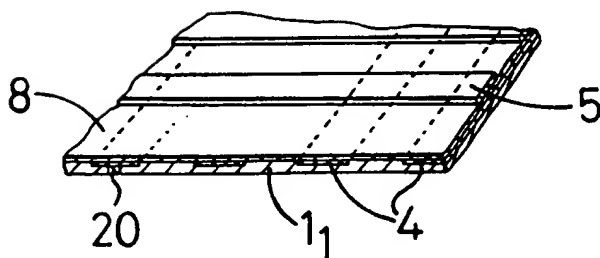
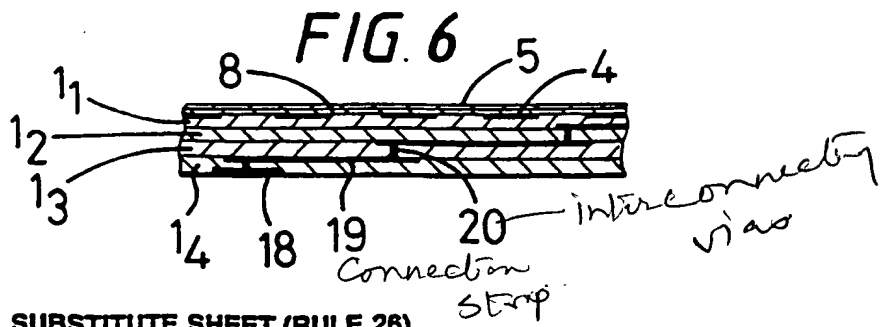


FIG. 6



SUBSTITUTE SHEET (RULE 26)

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FIG. 7

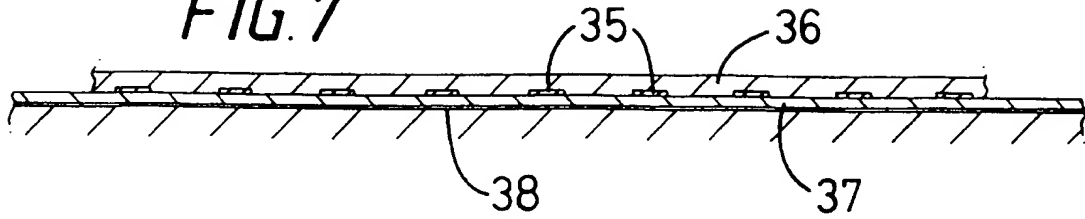


FIG. 8

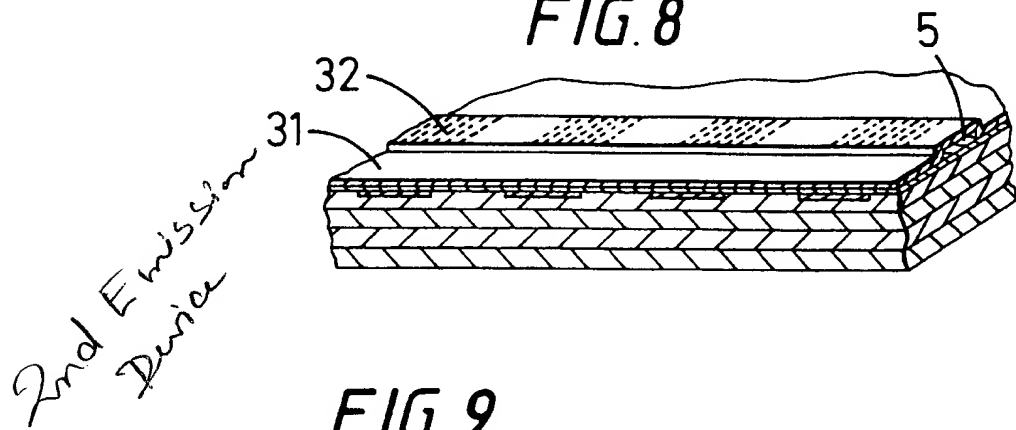


FIG. 9

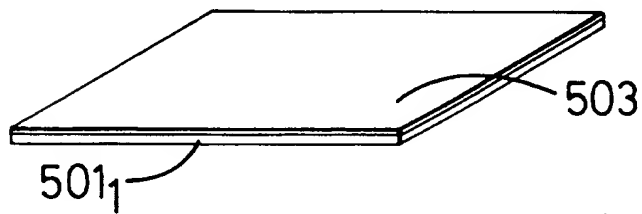
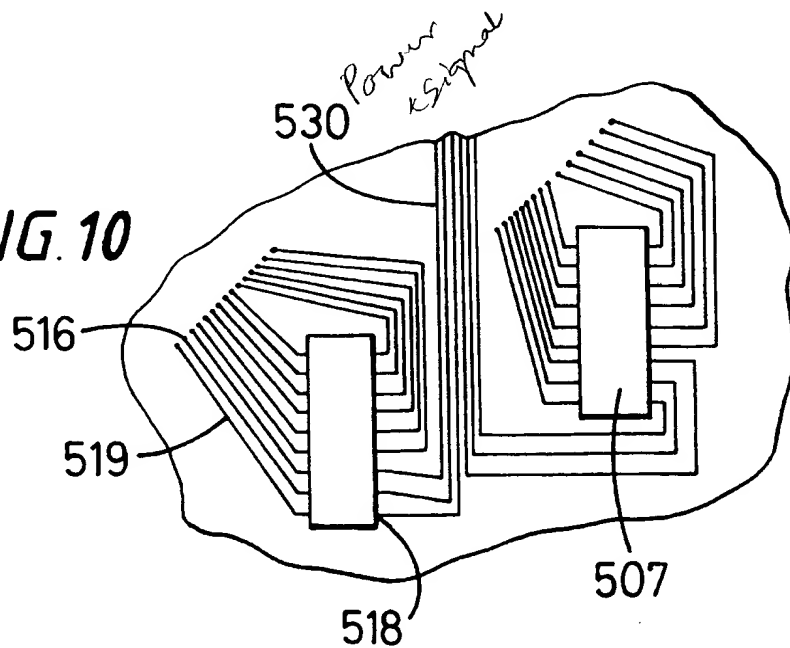


FIG. 10



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FIG. 11

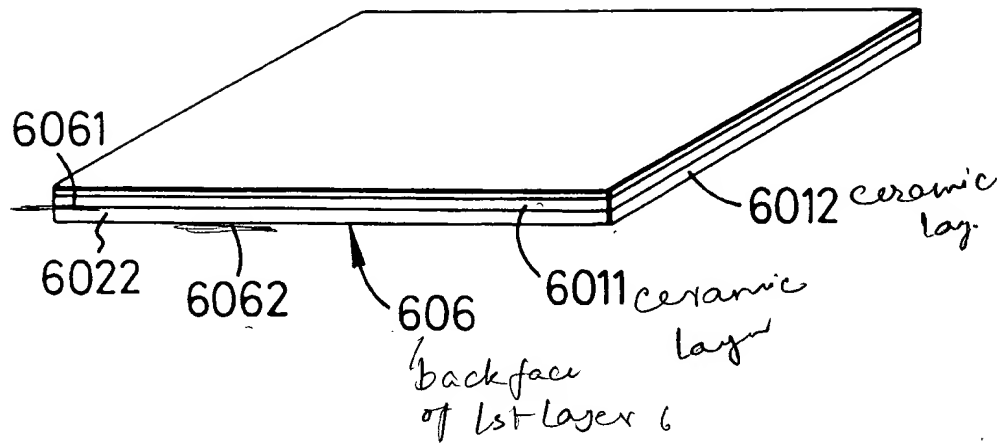
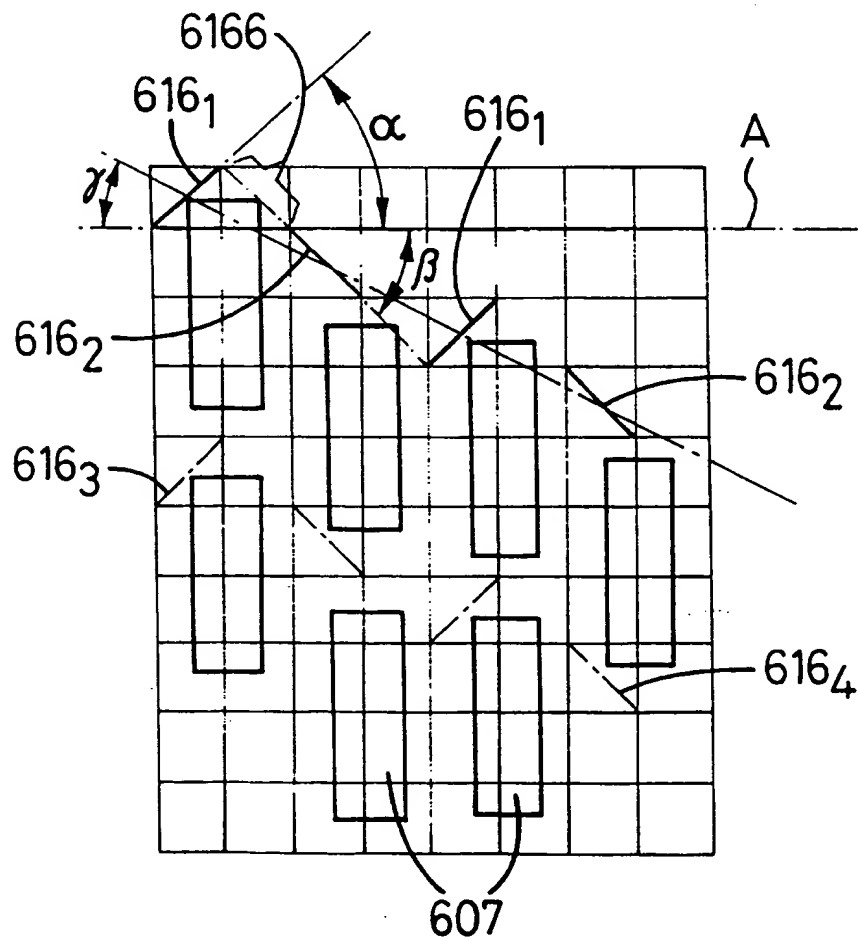
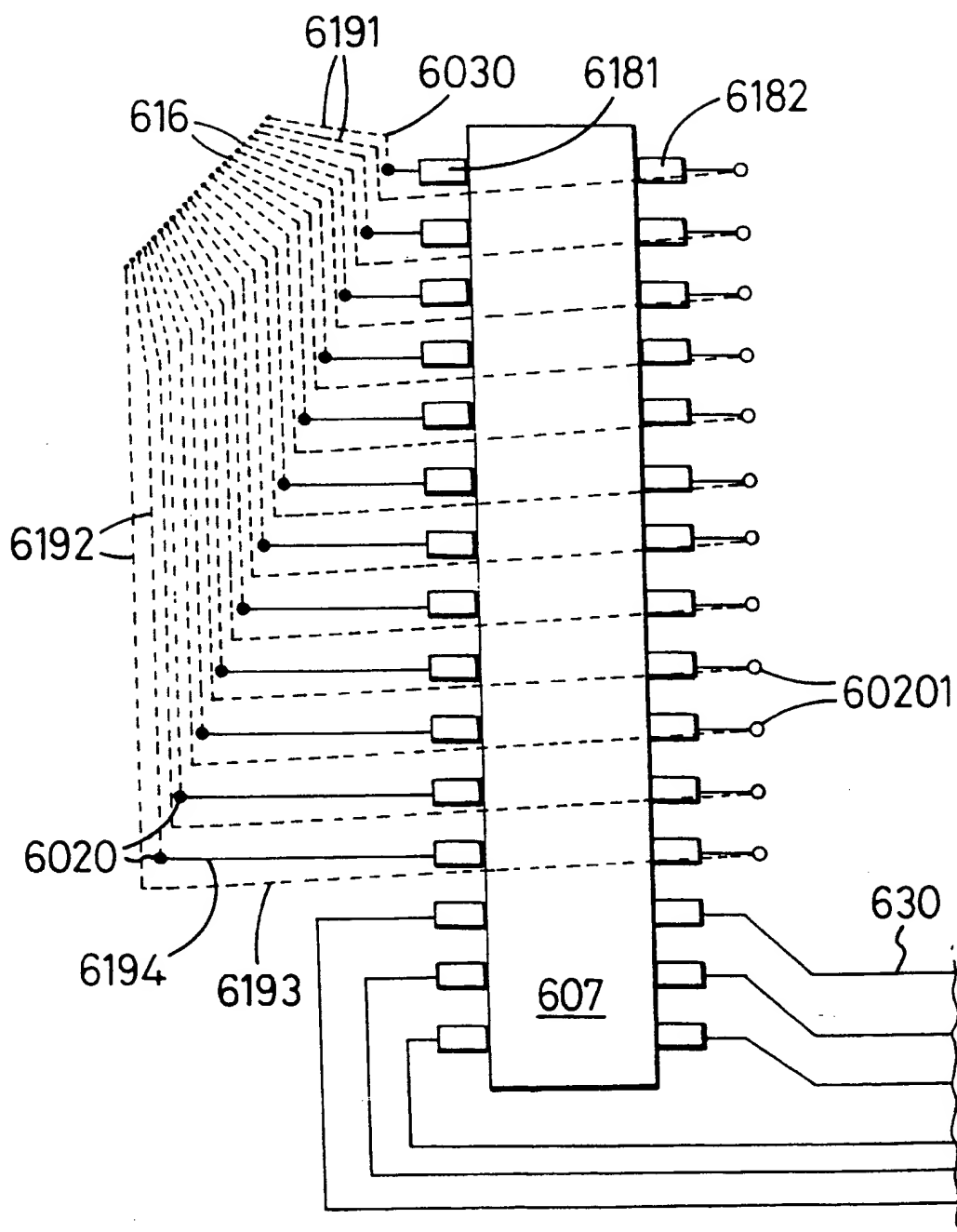
3rd Emission
Device

FIG. 13



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FIG. 12



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FIG. 14

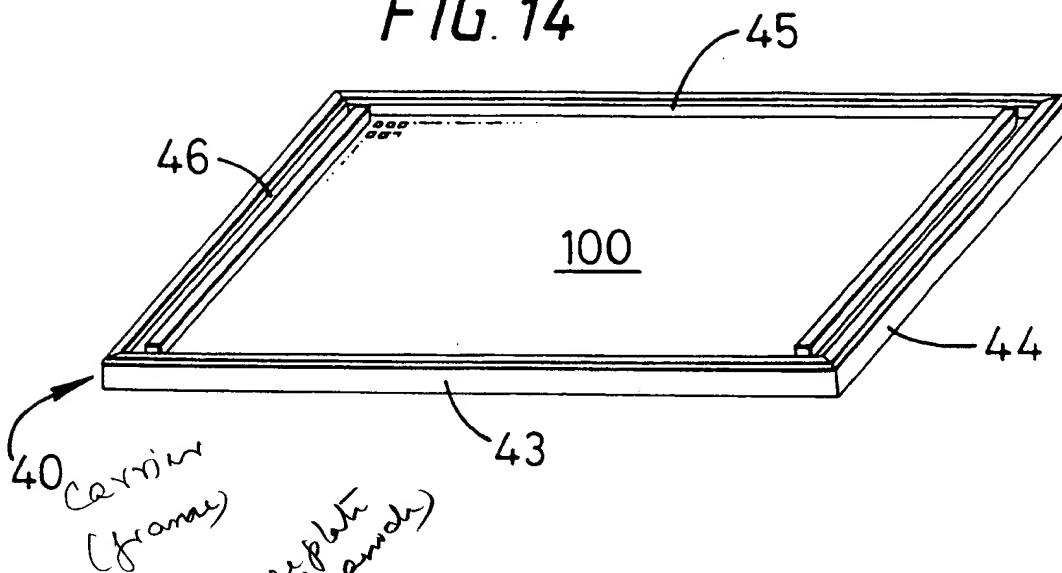
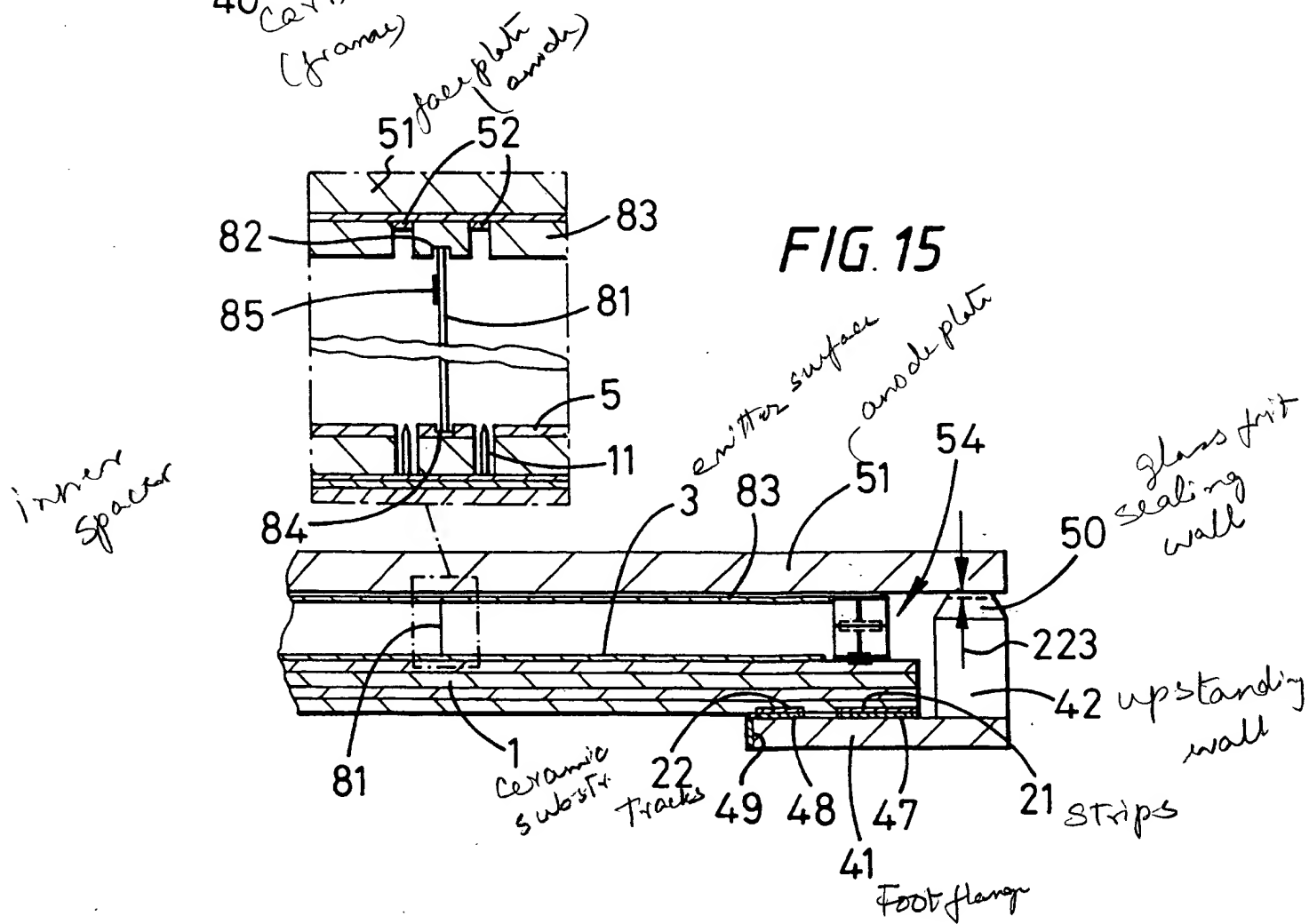


FIG. 15



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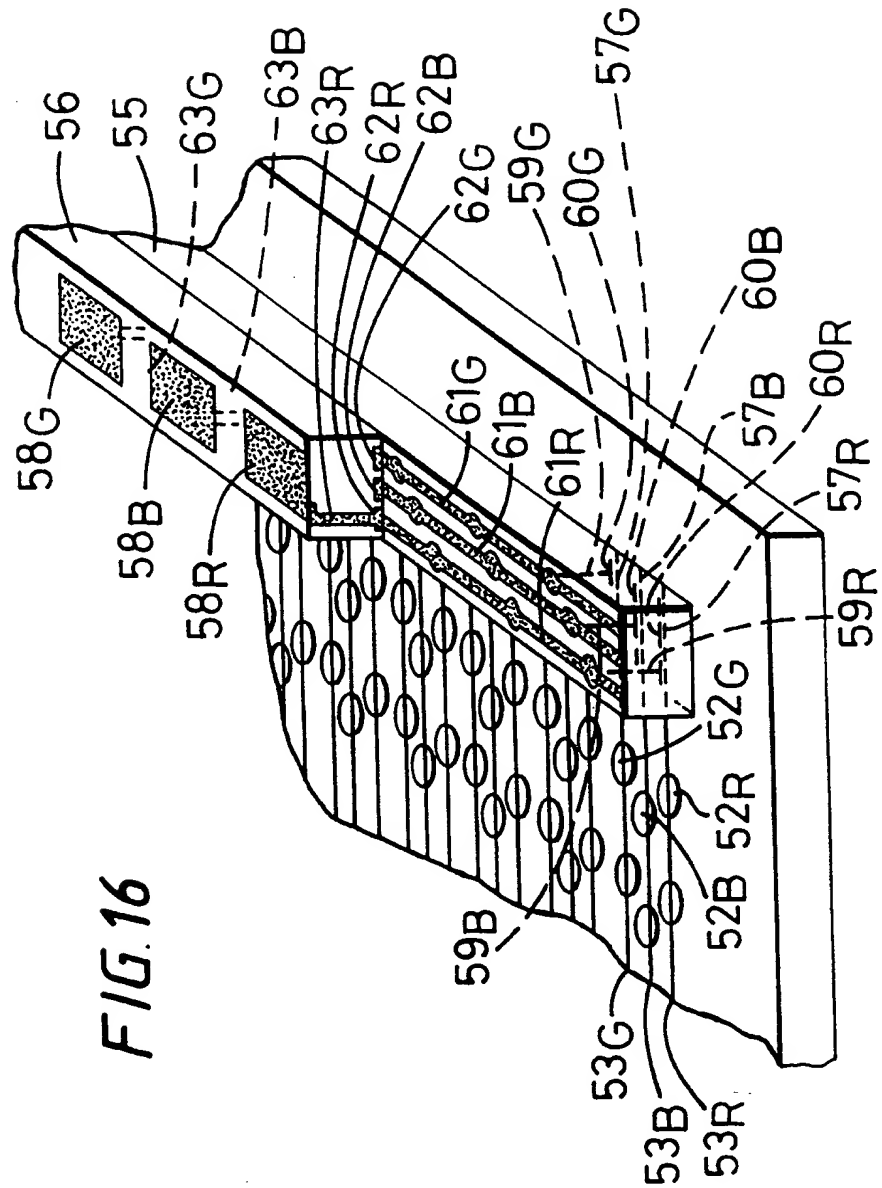


FIG. 16

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FIG. 17

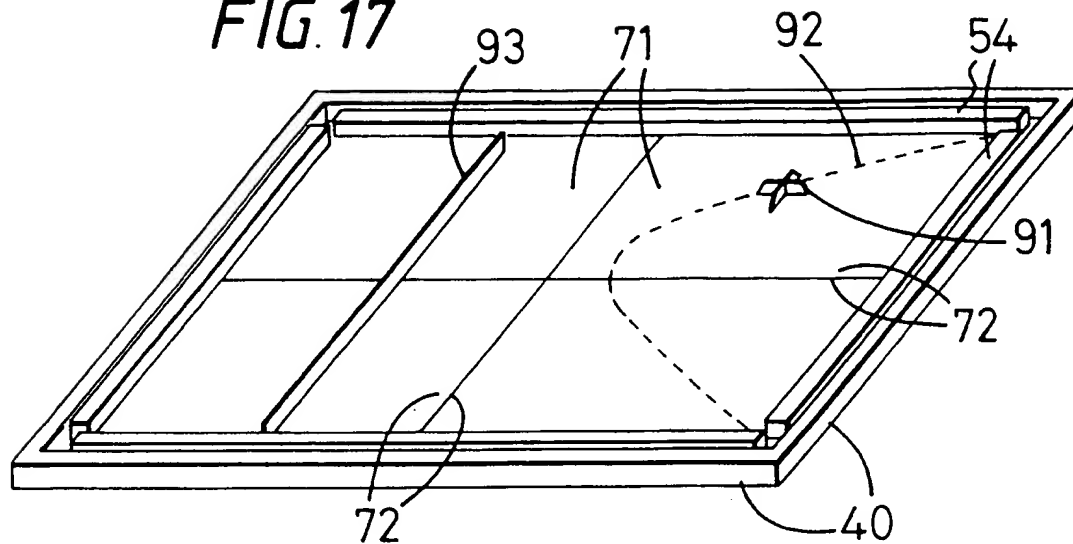
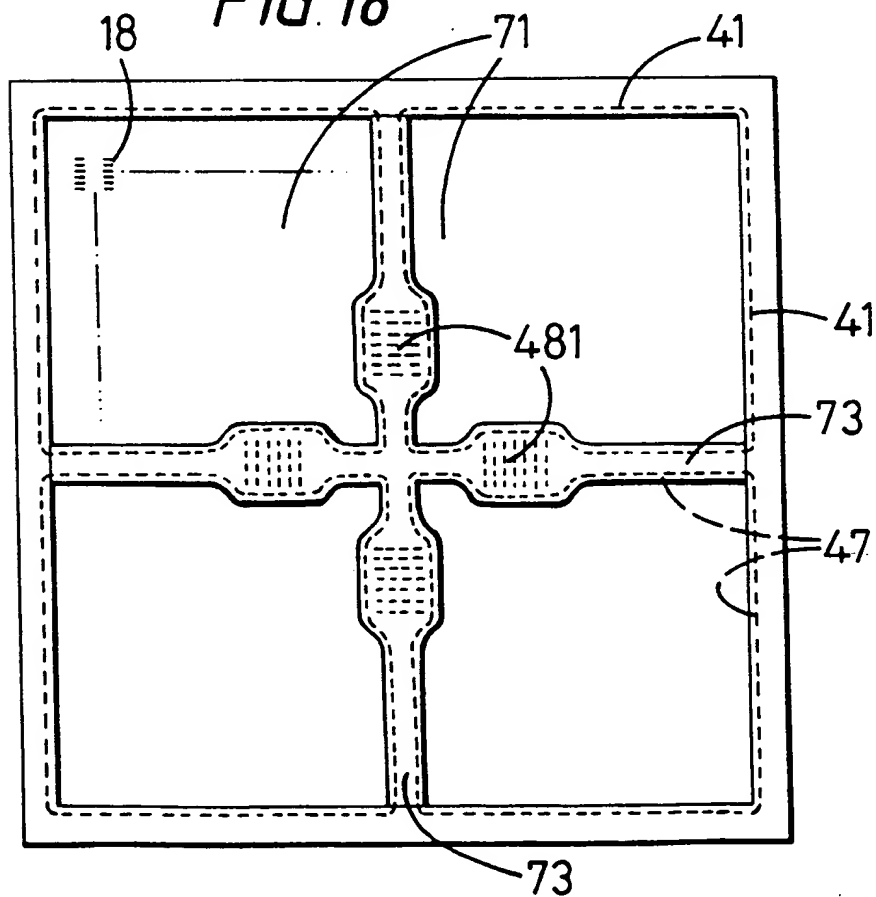
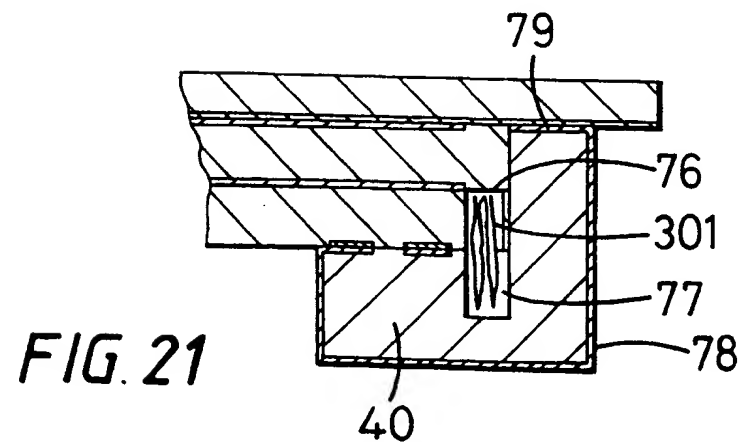
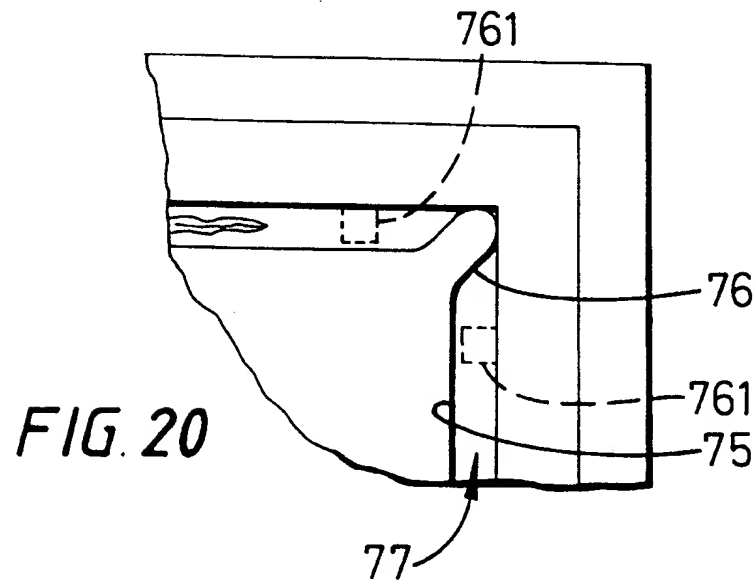
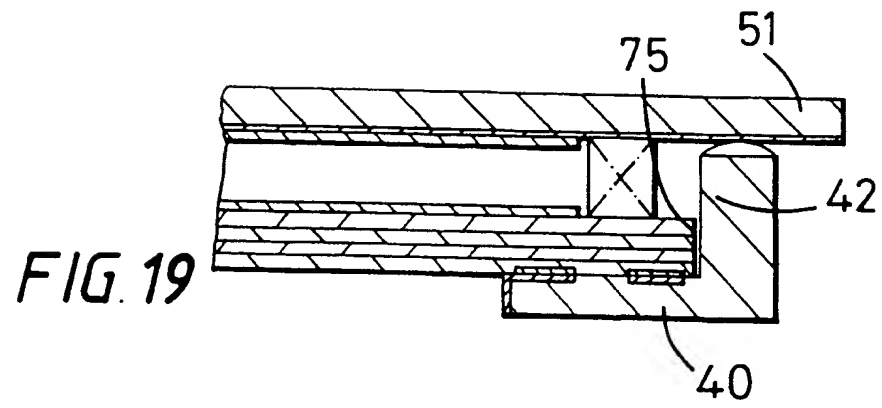


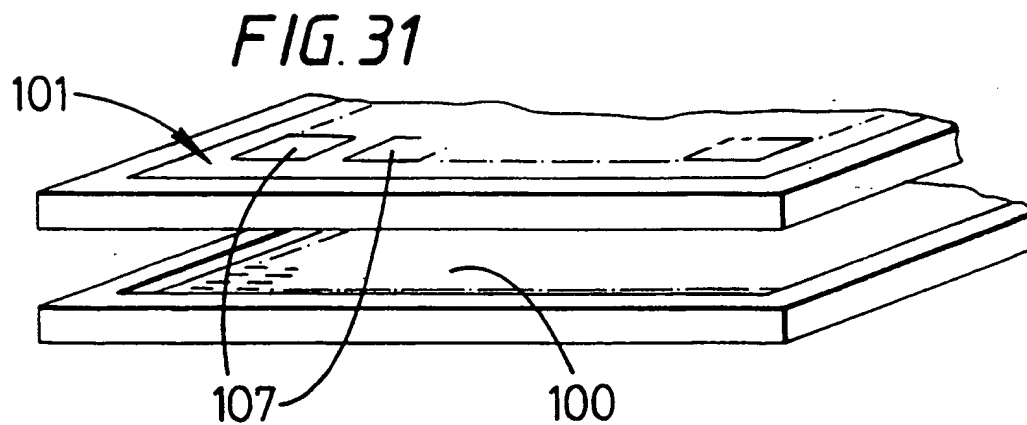
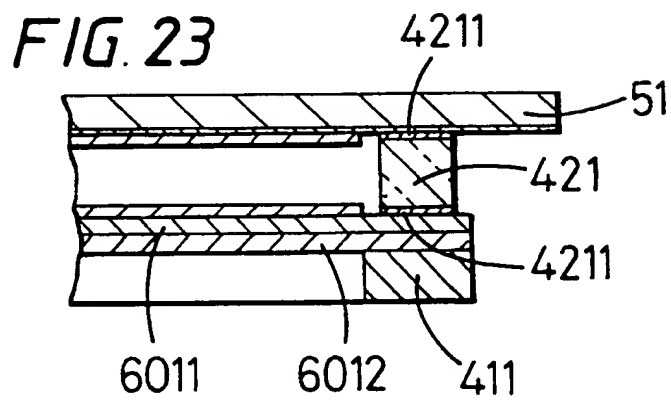
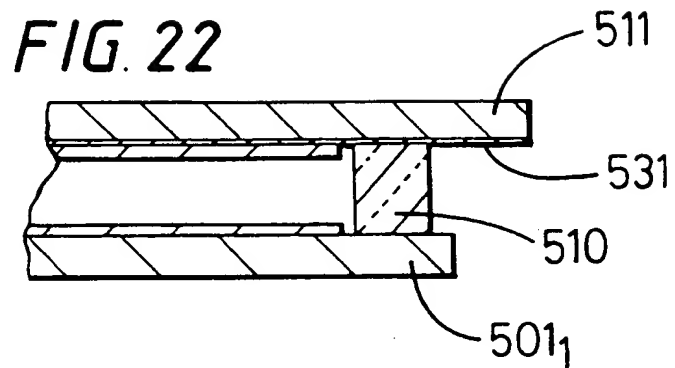
FIG. 18



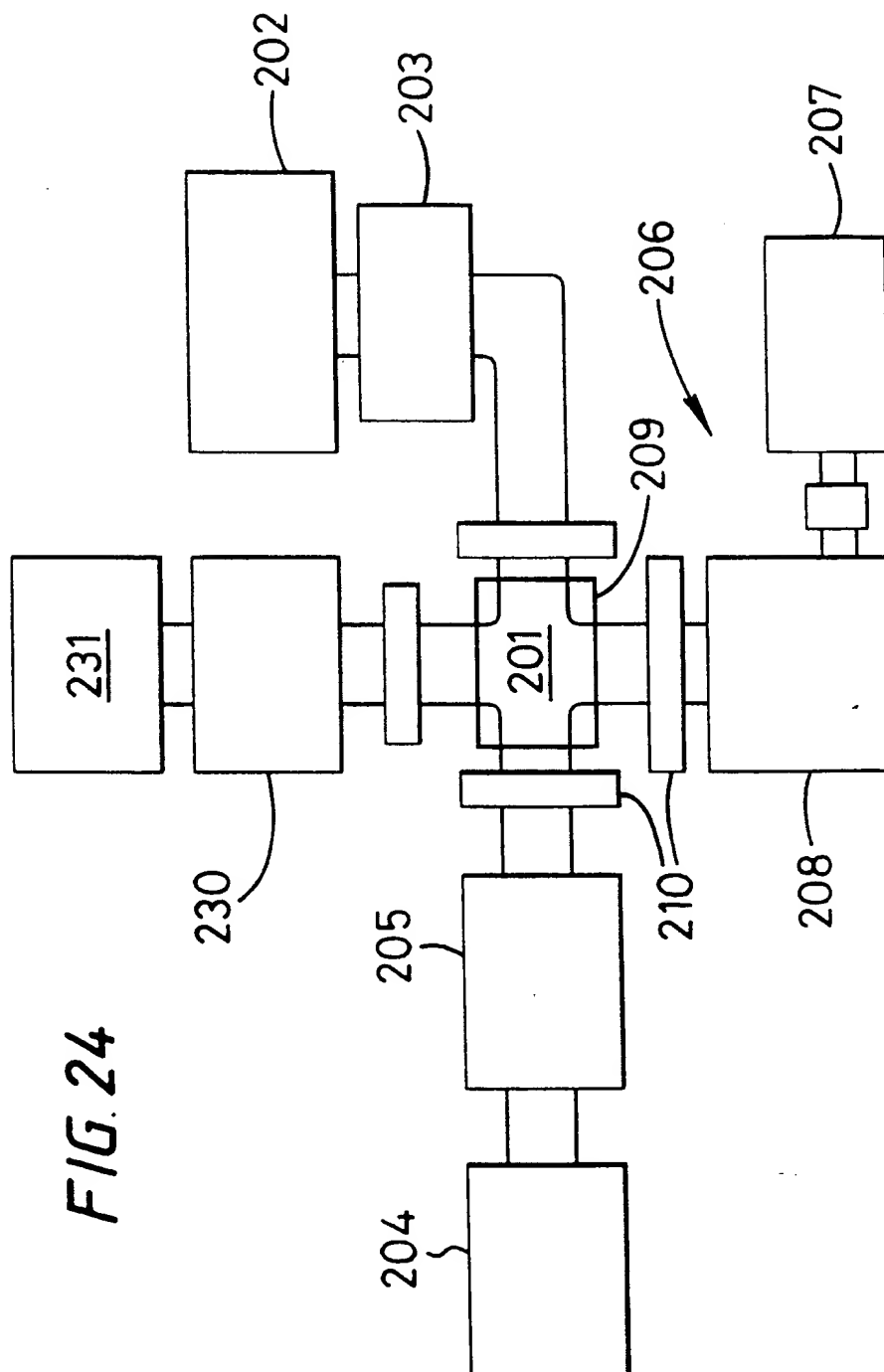
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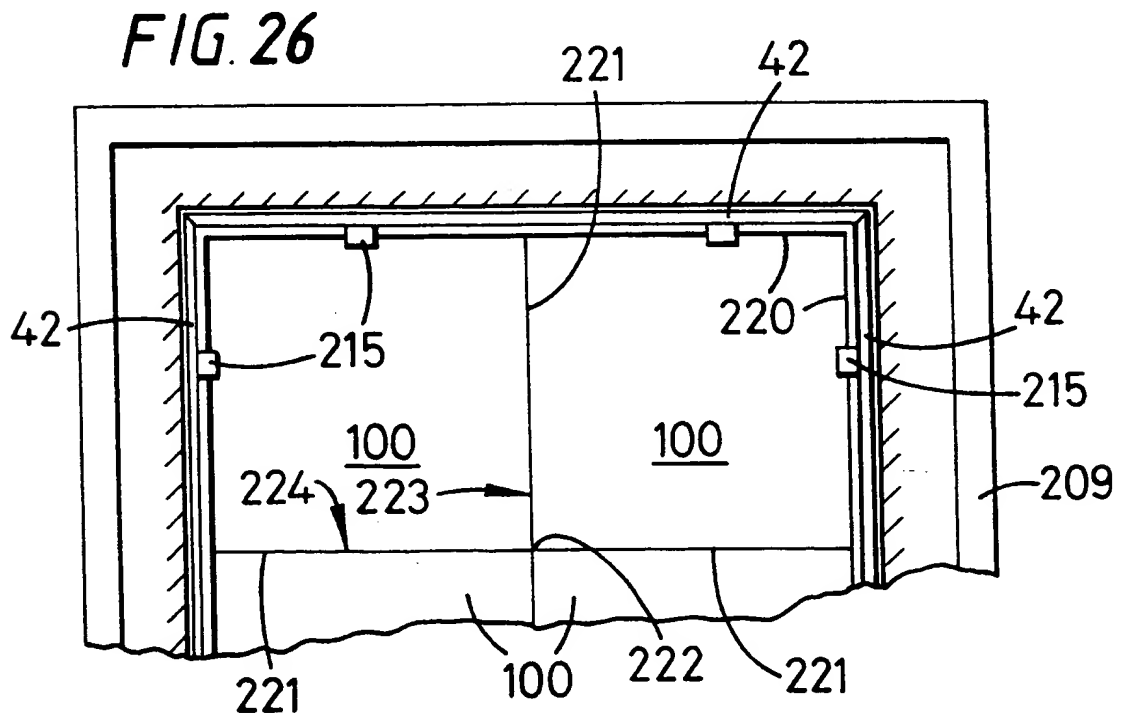
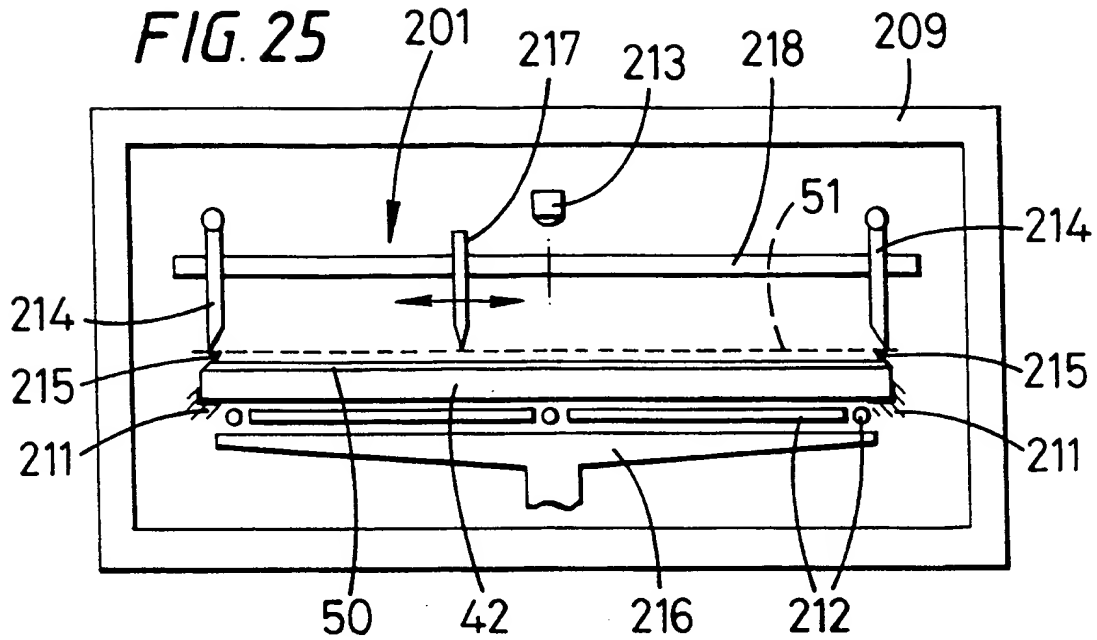
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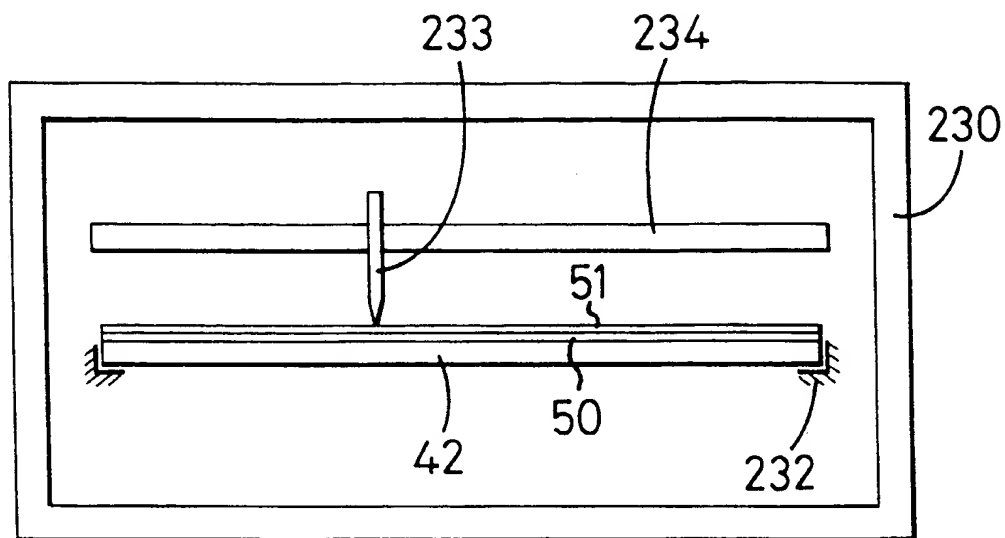


FIG. 27

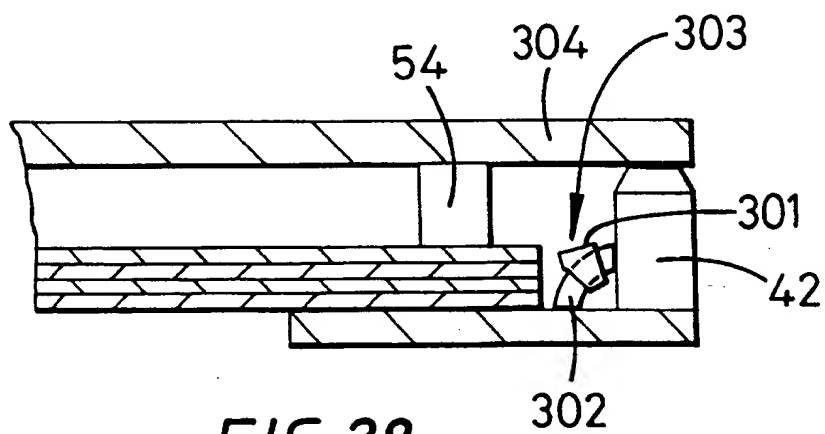
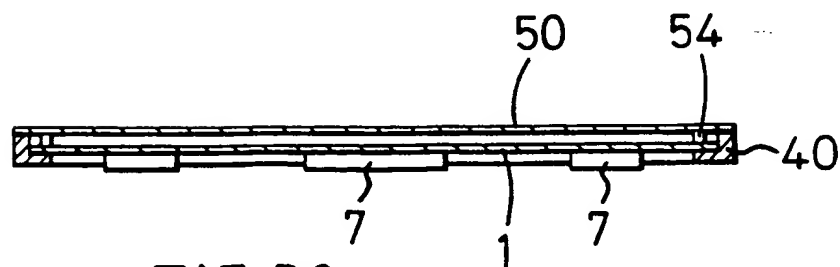
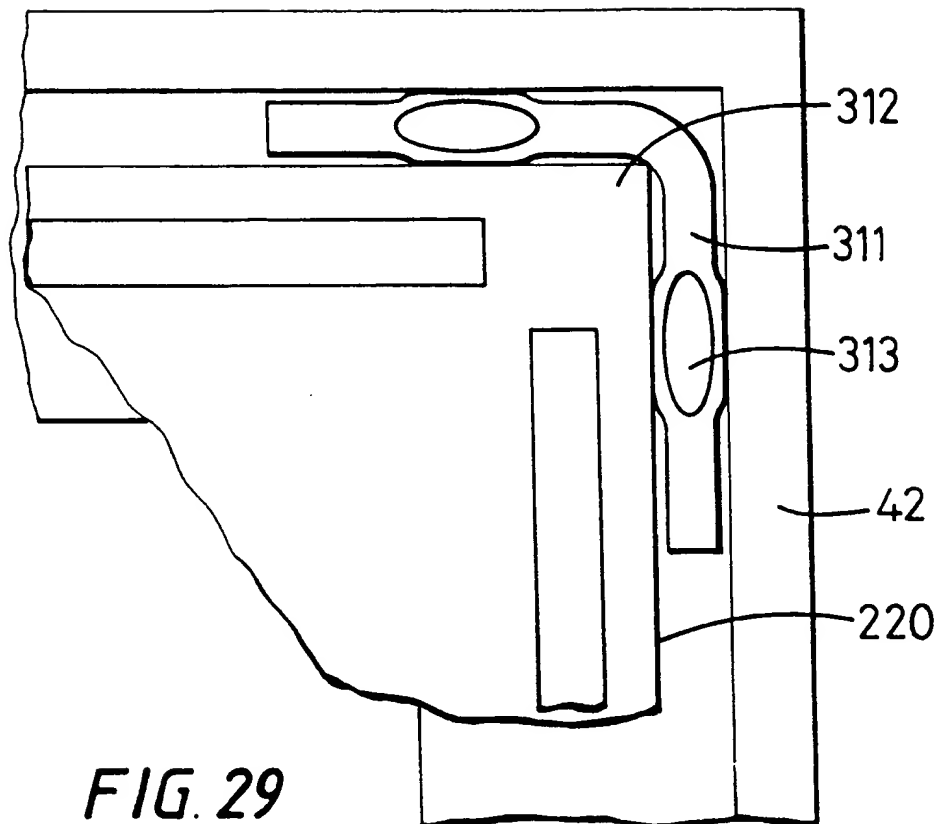
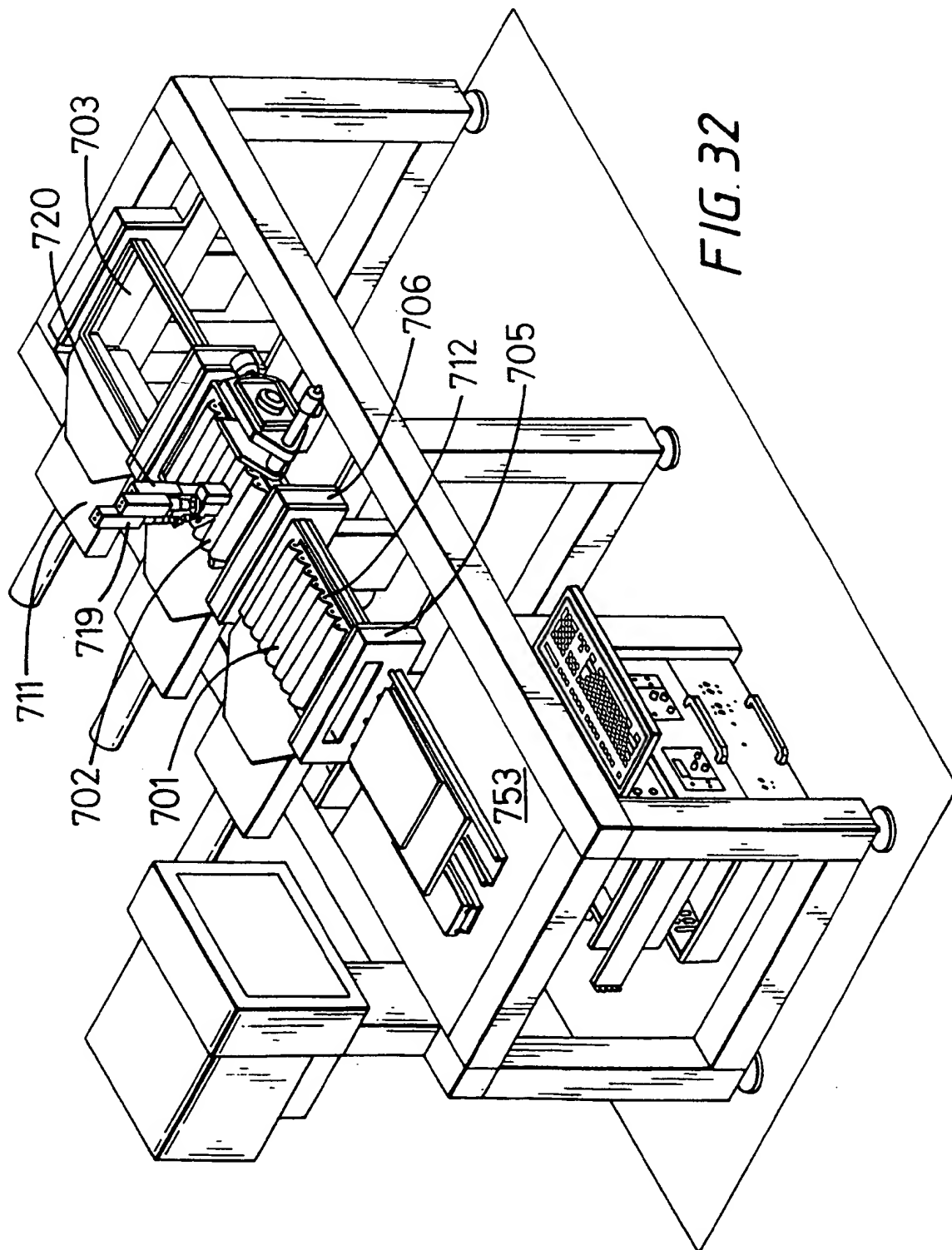


FIG. 28

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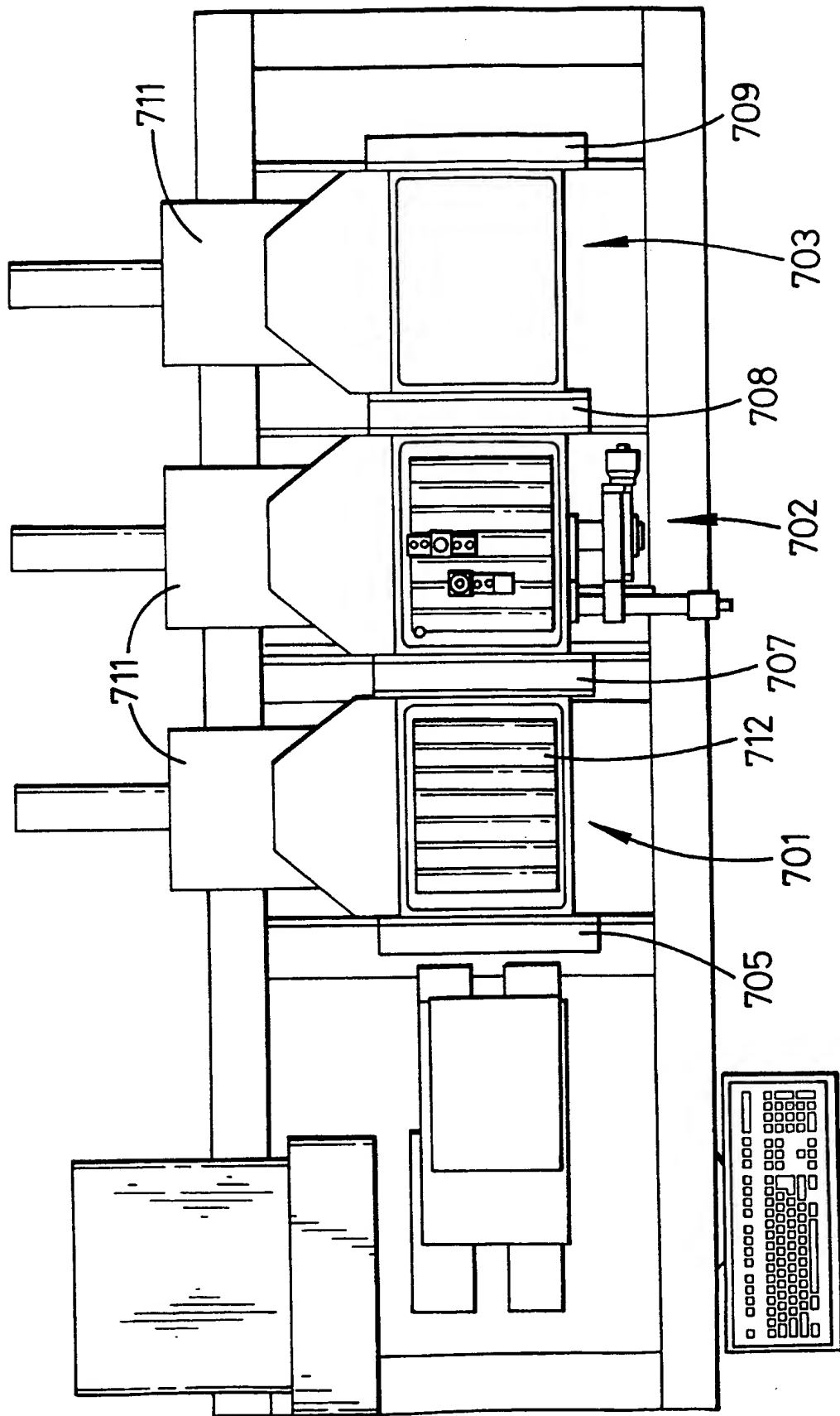
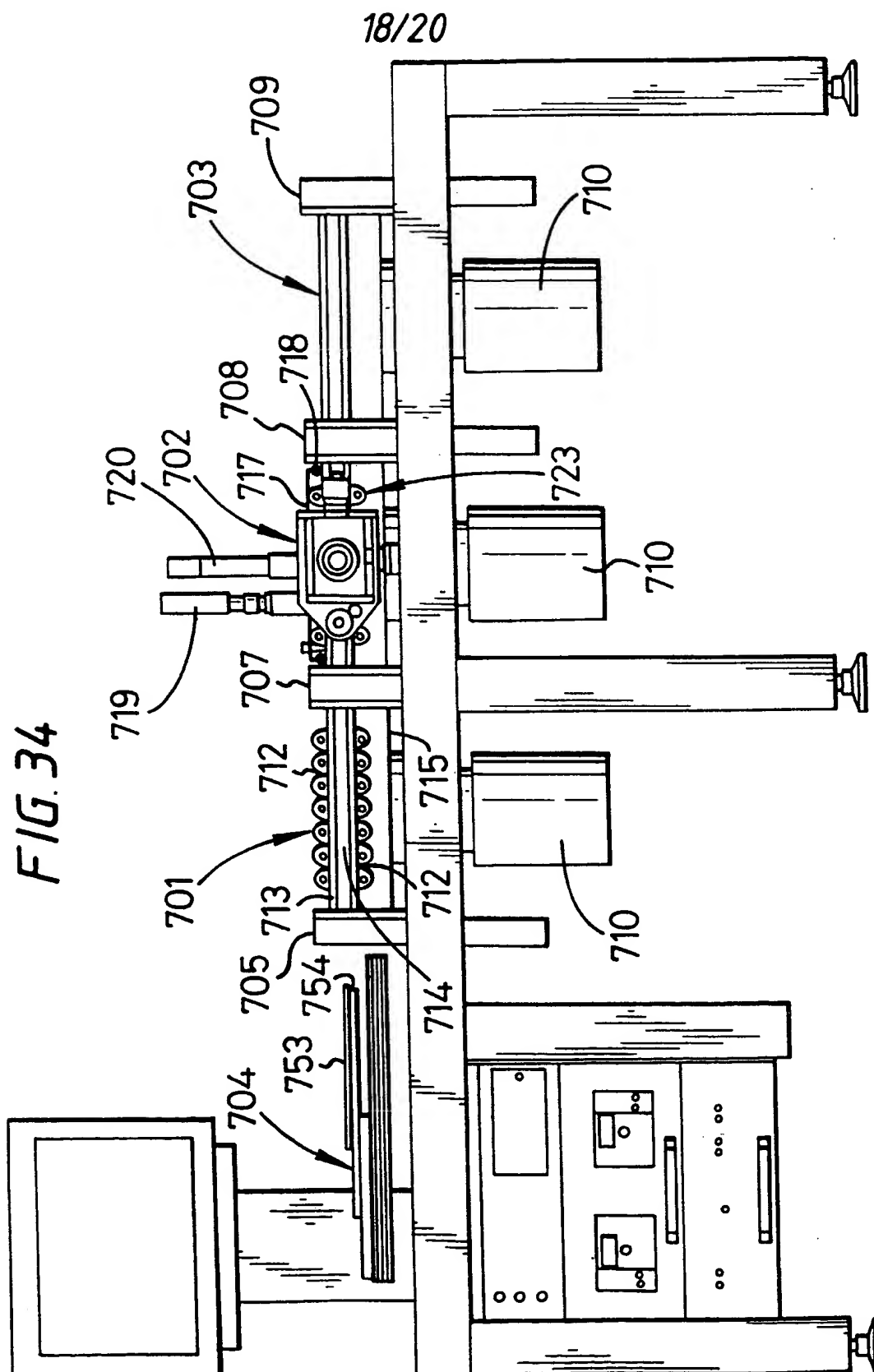
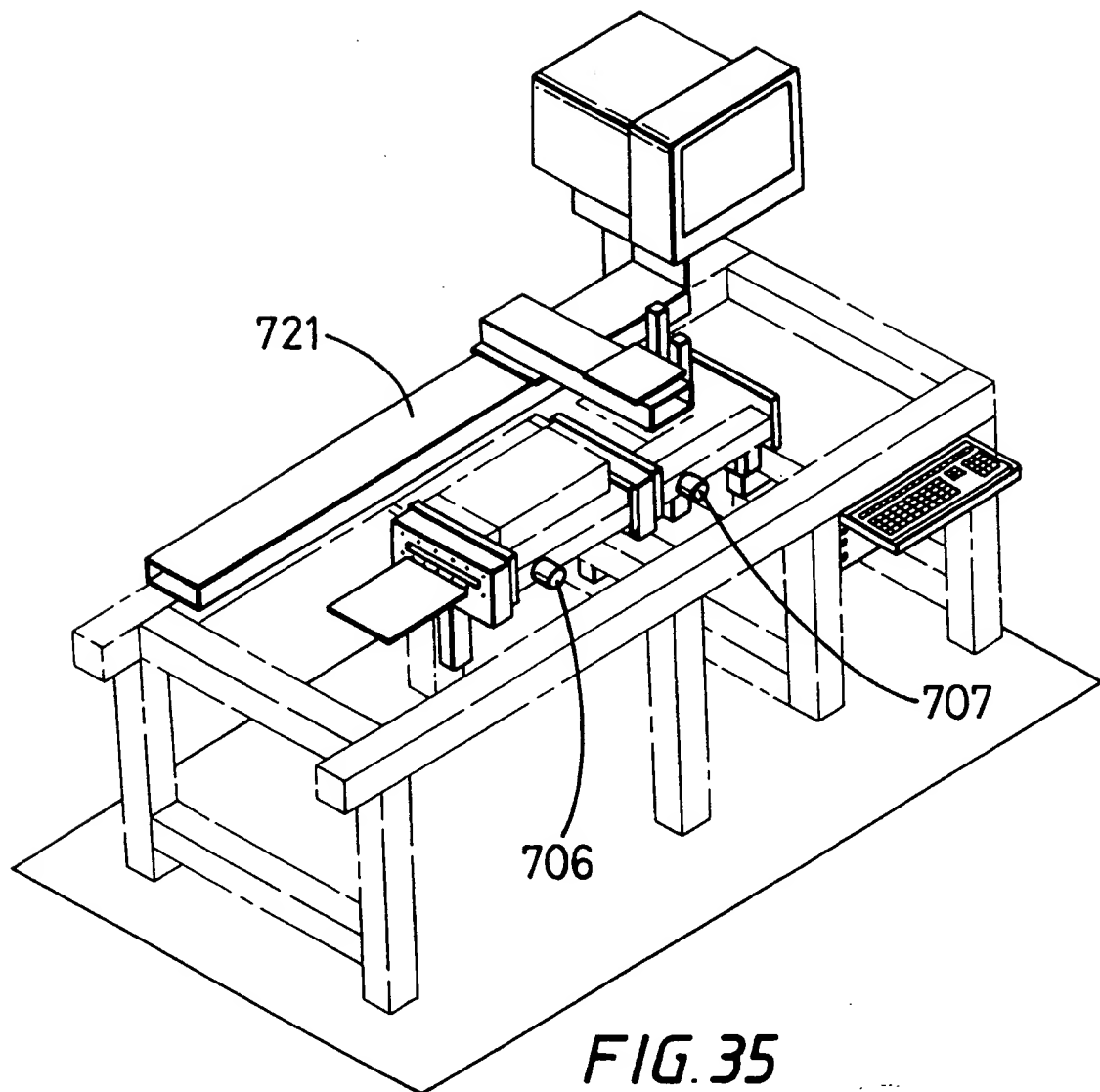


FIG. 33



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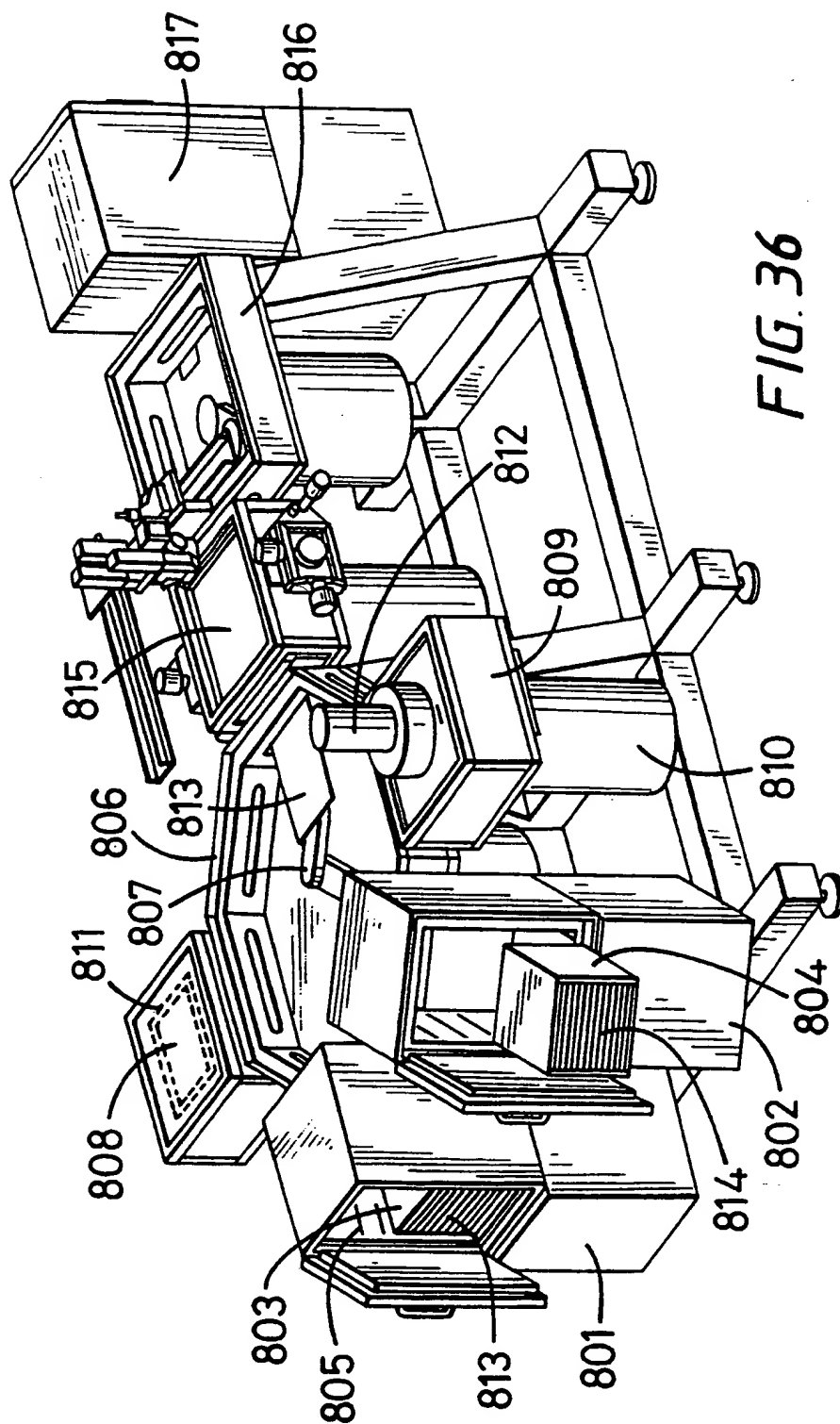


FIG. 36

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 98/20813

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H01J29/92

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	FR 2 697 660 A (PIXEL INT SA) 6 May 1994 see figure 1 see page 2, line 28 - line 33 see page 3, line 14 - line 26	1,2,5
Y	---	23,52
X	US 5 672 083 A (LOVOI PAUL A ET AL) 30 September 1997 see column 12, line 17 - line 63 see figures 2E,3	1,6
Y	---	23,52
X	WO 93 21650 A (SILICON VIDEO CORP) 28 October 1993 see page 29, line 21 - line 36; figure 4 -----	1,6

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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- "O" document referring to an oral disclosure, use, exhibition or other means
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Date of the actual completion of the international search

15 January 1999

Date of mailing of the international search report

22/01/1999

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INTERNATIONAL SEARCH REPORT

information on patent family members

International Application No

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